A

DISSERTATION REPORT

ON

THREE-LEVEL SINGLE INDUCTOR BRIDGELESS BOOST POWER FACTOR CORRECTION RECTIFIRE WITH VOLTAGE CLAMP PROPERTY

Submitted for the partial fulfilment of the requirement for the award of degree of

M-TECH DUAL

IN

ELECTRICAL ENGINEERING

With specialization in

POWER SYSTEM

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CERTIFICATE

I **ABHINANDAN ASHISH**, hereby certify that the work which is being presented in the seminar report entitled **"THREE-LEVEL SINGLE INDUCTOR BRIDGELESS BOOST POWER FACTOR CORRECTION RECTIFIRE WITH VOLTAGE CLAMP PROPERTY"** in partial fulfilment of the requirement for the award of M-TECH DUAL DEGREE in Power System and submitted in the department of Electrical Engineering of the **SURESH GYAN VIHAR UNIVERSITY, JAIPUR** is an authentic record of my work under the supervision of **Mr. M SASHILAL** Head of Department of Electrical Engineering and in the guidance of Asst. Prof. **Miss. VISHU GUPTA.**

The matter presented in the report embodies the result of own work and studies carried out by me is have not been submitted for the award of any other degree of this or any other university.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Date:

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I am feeling so, proud and lucky on completion of my dissertation work . and it comes true only by blessing of god.

So, first of all i would be thankful to that supernatural power who giving me the strength and opportunity to do this work.

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ABSTRACT

In power system power factor (p.f) is an important factor of continuous quality electrical supply some time it reduces due to some reactive power disorder power factor affected and by hence the quality (voltage and efficiency) also affected.

There are many methods to improve the power factor such as capacitor bank, synchronous condenser, thyristor controlled rectifier(TCR) etc. But they have losses problem so a new technique is introduced three level single inductor bridge less boost power factor correction rectifier with voltage clamp property by the MATLAB simulation technique it used bridge less three level boost topology.

It consist of two different types of diode, i.e fast diode & slow diode , MOSFET, capacitor & inductor due to use of semiconductor device soft switching it has high efficiency, low device voltage stress as well as high Voltage gain.

With the help of MATLAB simulation four modes of operation is processed these are (a).Charging stage in the positive half cycle and (b).discharging stage in positive half cycle (c).Charging stage in the negative half cycle and (d). Discharging stage in negative half cycle and the whole improved power factor supply is obtained in the wave form. And this output is to give the feasible input to the other electrical device such as electrical motor. It can be used in UPS for regular power supply.

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CHAPTER 1

INTRODUCTION

Electricity is the backbone of the economy and development of any country it is useful in every part of life i.e irrigation, lighting, infrastructure development and the country's security point of view.

And for a quality electricity or power a suitable power factor is very essential for the supply of electricity in this report we have discussed on every point of power factor and its correction by the soft switching method over the conventional method of power factor correction.

We have discussed about the single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp. This method is based on the soft switching & switched mode power supply (SMPS).

1.1 Introduction of power factor.

Generally people relate the electricity in KW but this is not the complete introduction of electricity it is the only part of it.

Broadly electricity can be divided in three parts.

(a). Apparent power (unit volt-ampere)

(b). Real power (unit watt)

(c). Relative power (unit VAR).

Apparent power can easily be calculated & measured and this is the product of the single-phase RMS voltage and current.

$$A.P_S = V_{rms} \times I_{rms}$$

And these three power are influenced by the factor called power factor. the correlation between real and reactive power consumption is known as power factor .

$$\textbf{Power Factor} = \cos(\varphi) = \frac{P_{(kw)}}{S_{(kvA)}}$$

1.2 Correction of Power Factor.

Power factor is altered by the increment or decrement of active and reactive power this can be corrected through different method these are as follows.

(a). Conventional method.

(b). Soft switching method.

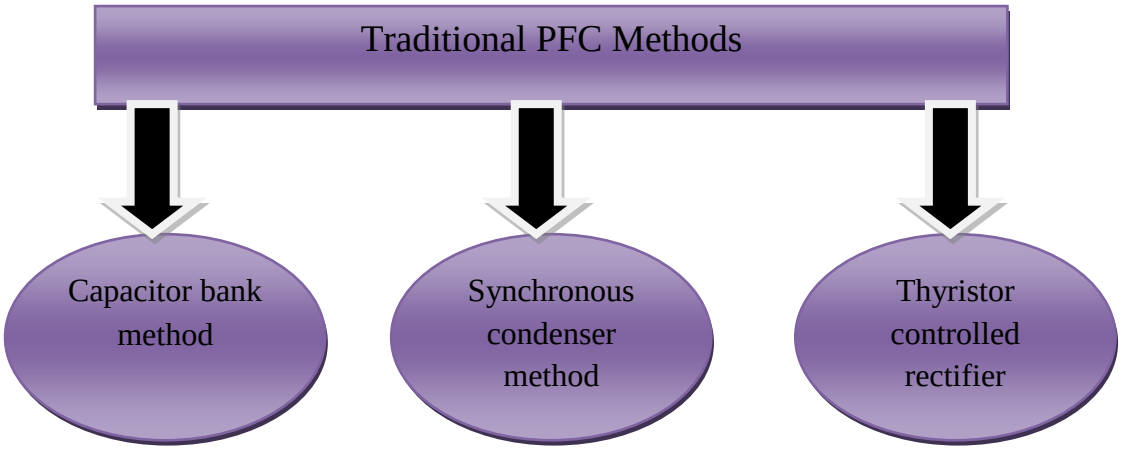

Fig.1.1. These are the mainly three conventional methods of PFC correction

Capacitor Bank:

In this method a capacitor bank is connected across the load. We know that the capacitor takes the leading reactive power and by hence the leading reactive power and by hence the overall reactive power taken from the source decreases resulting the system power improves.

Synchronous Condenser:

When a three phase synchronous motor working in over excited mode then actually it is working as synchronous condenser or as a capacitor. Synchronous condenser gives the dynamic power factor correction over a huge area of excitation.

In under excited condition synchronous motor working in lagging power factor and hence it absorbs the reactive power from the source but in over excited condition it works in leading power factor and hence it generates the reactive power & works as a capacitor. A static capacitor bank provides discrete power factor control but the synchronous condenser has continuous power factor control .

Thyristor Controlled Rectifier:

Static thyristor controlled reactors are the major components static VAR compensator. Static thyristor controlled reactors is connected in parallel way with load for control of the reactive power flow.

1.3. Effects of Poor Power Factor:

Poor power factor results falling quality power supply and introduction of harmonics. Non-linear load in power system products voltage and current harmonics which

decreases the efficiency and increases losses, which gives negative impact on electrical power supply.

There are Mainly Two Types of Power Factor Situation:

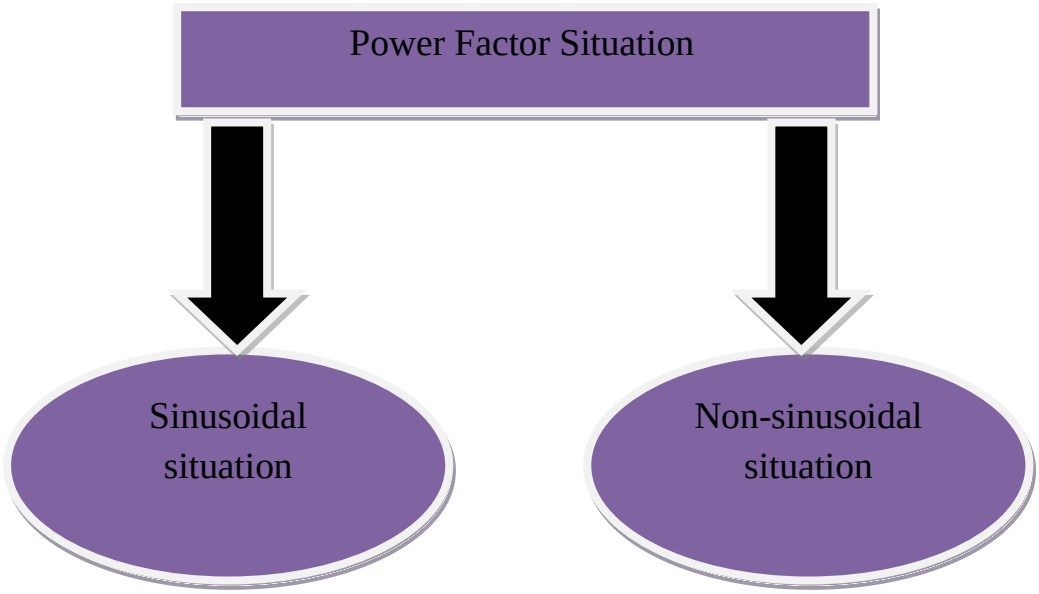

Fig.1.2 both are the situation of power factor

For non sinusoidal situation:

The voltage load and the current loads are.

$$V(t) = V_1 \sin(\omega_0 t + \delta_1) \qquad (1)$$

$$I(t) = I_1 \sin(\omega_0 t + \theta_1) \qquad (2)$$

Where V_1 & I_1 are the peak value of 60/50 Hz voltage current and δ_1 and θ_1 are there phase angles.

$$TDH_v = \frac{\sqrt{\sum_{K=2}^{\infty} V^2 K_{rms}}}{V_{1rms}} \times 100\% = \frac{\sqrt{\sum_{K=2}^{\infty} {V_k}^2}}{V_1} \times 100\% \qquad (3)$$

$$TDH_I = \frac{\sqrt{\sum_{k=2}^{\infty} V^2 krms}}{I_{1rms}} \times 100\% = \frac{\sqrt{\sum_{k=2}^{\infty} I^2 k}}{I_1} \times 100\% \qquad (4)$$

Where TDH stands for the total harmonic distortion.

So, it is to be clear that the power factor and the total harmonic distortion are clearly related.

1.4 Negative Aspects of Poor Power Factor:

Due to some additional non-linear load it is the power factor which gets lagging or poor gives birth to many un wanted problem which drops the quality of power.

And these problems are as follows:

(a). It drops the quality of supply voltage.

(b). It drops the quality of supply current.

(c). It increases the harmonics in voltage and current.

(d). It increases the output losses.

(e). It decreases the efficiency of output of the electrical machine.

(f). It affects the life of electrical appliances.

1.5Advantages of Corrected or Improved Power Factor:

(a). It improves the quality of electrical power supply.

(b). It extracts the voltage and current harmonics.

(c). Efficiency increases.

(d). Life of the electrical appliances also increases.

1.6. Power Factor Correction by Three-Level single inductor Bridgeless Boost Converter with Voltage Clamp Property:

This type of converter has very high output efficiency due to the soft switching technique and to give the further detail of the circuit we will have to discuss about soft switching.

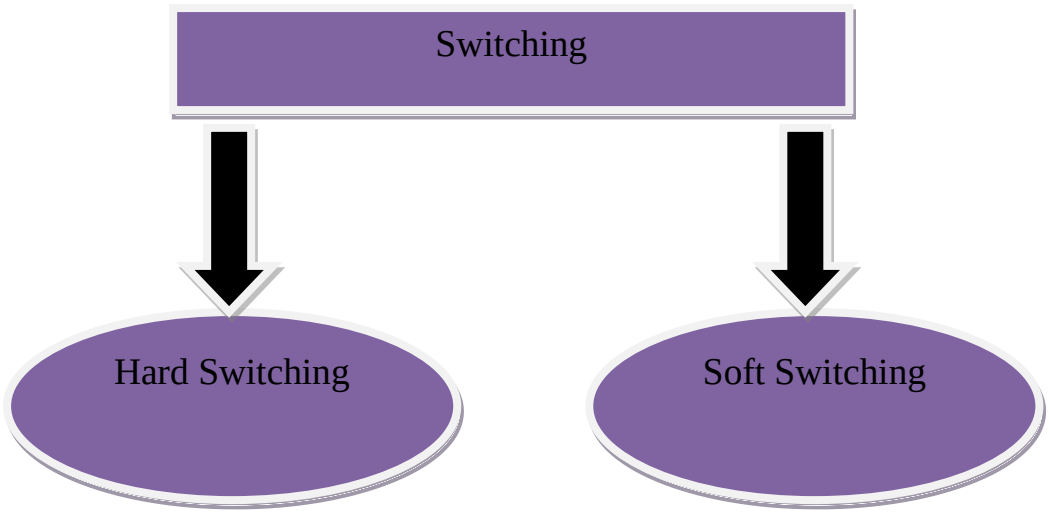

Fig.1.3. These are mainly two types of switching

1.7. Hard Switching:

Hard switching are the conventional switching which is heavy, complex, costly & larger in size as well as it has some drawbacks of loss of electrical power & lower output efficiency because it consumes as well as stores some power which affects the output electrical efficiency. And these draw backs gives birth to the concept of soft switching.

1.8. Soft Switching:

To overcome the drawbacks of hard switching, soft switching technique is introduced. In this type of switching semi-conductor power electronics switches are used. in this concept two types of switching is done.

(a). Zero voltage switching

(b). Zero current switching

Zero Current Switching.

In zero current switching IGBT is used in which when current becomes at zero value then the circuit gets switched of and by this type of turn off method there is no loss in electrical power and by hence its efficiency is enhanced.

Zero Voltage Switching.

In zero voltage switching the MOSFET is used as a power electronic switch in which switch voltage is brought to zero volt gate pulse is applied in gate terminal of switch after that smooth turn ON is achieved with eliminated switching loss.

1.9. What is Single Phase Topology (based on boost converter)?

The requirement of solid state ac-dc converter for the improvement of power quality from the power factor correction point of view it reduces the total harmonic distortion at input in ac mains. And gives the smooth dc output and this need motivate the several topologies based on the power electronics converter.

i.e buck, boost and buck-boost. The mode of operation of boost converter is continuous current mode (CCM) is become popular due to reduction of electromagnetic interface (EMI).

The evolution of the traditional boost converter is elaborated in terms of enhanced characteristics achieved by other topology based on boost converter.

The conventional boost converter for the power factor correction is not more reliable and efficient because of losses and complex construction generates a need of new invention for the power factor correction which will more efficient and simple in construction, faster in switching and the most important beneficial in terms of economy and now for this a new concept is introduced called single inductor three-level bridge

boost power factor correction. in next page we will discuss about the three level bridge less power factor correction which is designed on MATLAB simulation.

1.10. Three Level Single Inductor Bridgeless Boost PFC With Voltage Clamp Property.

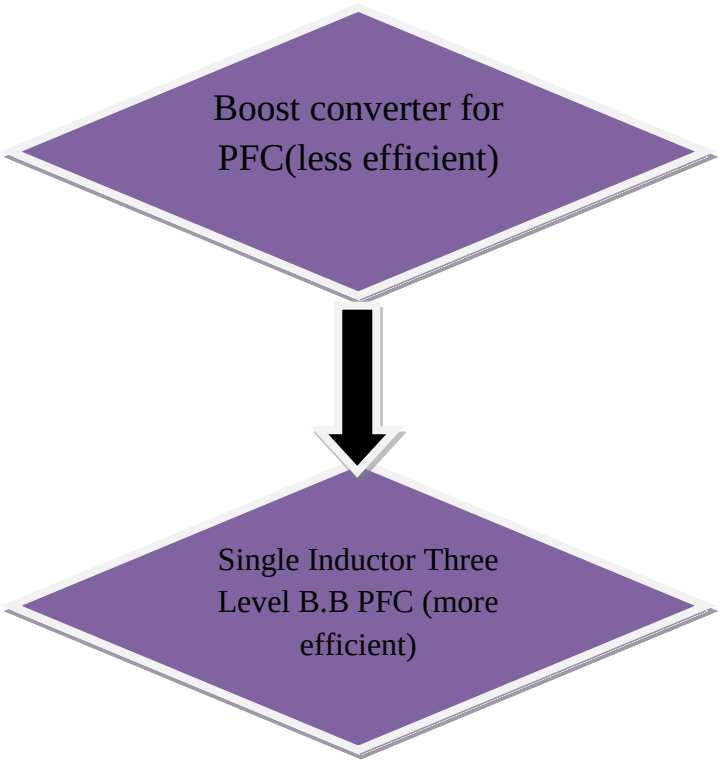

Fig.1.4. shows the difference between conventional and new bridgeless rectifier converter.

Earlier the dual boost power factor correction rectifier is a good topology with full utilization of of two MOSFET but its drawback is high conduction noise .

After that the totem pole boost bridgeless power factor rectifier is introduced with lower conduction mode (CM) noise but some drawback of reverse recovery characteristics of MOSFET don't gives it continues current mode (CCM) operation. To remove its draw back a new bridgeless power factor correction with two boost converter circuit replacing the switch leg is used to replaced the conduction of MOSFET body diode and it can also operate in continues current mode (CCM) but in this circuit a floating gate driver with extra inductor is required which makes it heavier.

After that a bidirectional boost bridge less power factor correction rectifier is introduced with bidirectional switches. But it also suffers from conduction mode (CM) noise. To replace all these demerits and drawbacks the single inductor with three-level bridgeless boost PFC rectifier is introduced. in this converter two slow diode is are working as rectifier diode as well as clamping diode simultaneously. The slow

diode and the intrinsic diode of MOSFET operates with switching frequency and replace the problem of reverse recovery, nature voltage clamp has achieved and voltage stress of the devices becomes half of the output voltage.

Advantages of the Converter

(a). Only one inductor is required.

(b). Low device voltage stress with the nature voltage clamp.

(c). Voltage stress low and reduction of conduction losses and low CM noise interference.

(d). Utilization factor of the semi conductor device becomes high.

Steps of Changes Comes In PFC Converters.

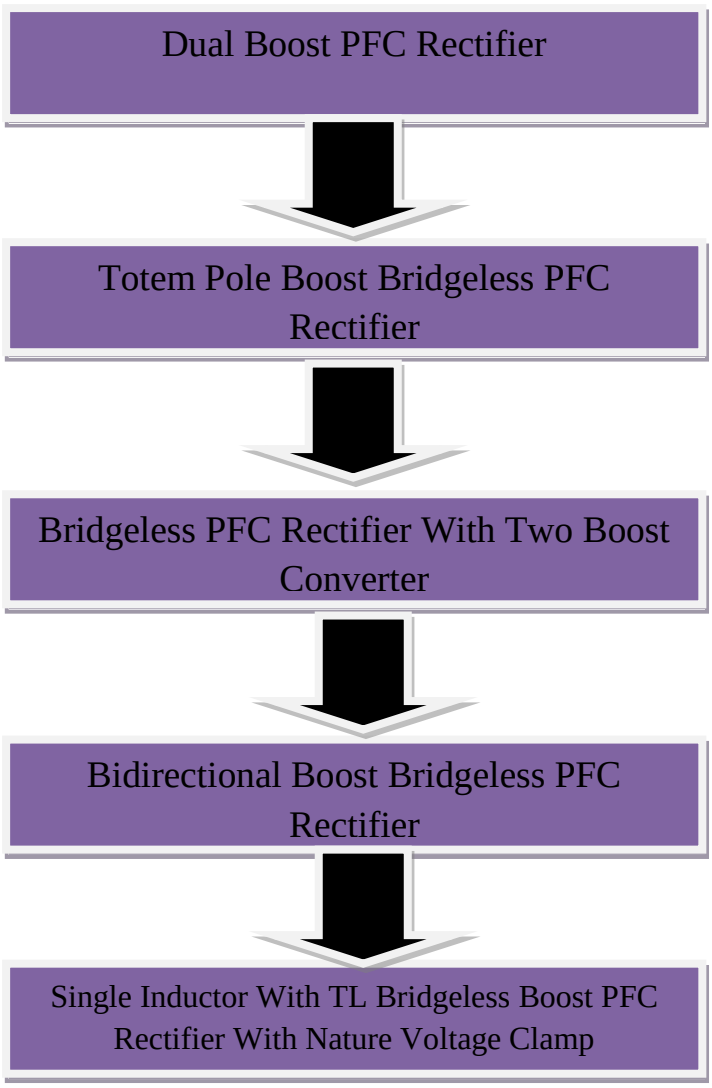

Fig. 1.5 Story of development of the single inductor with TL Bridgeless boost PFC rectifier with nature voltage clamp.

CHAPTER 2

OPERATIONAL ANALYSIS

In this chapter we will discuss about the working principle and the structural detail of the proposed converter circuit. Different mode of operation is discussed in this section.

To solve the problem remain in the three level bridgeless boost power factor correction with only one inductor is proposed in this given circuit. Its description is given in the figure below.

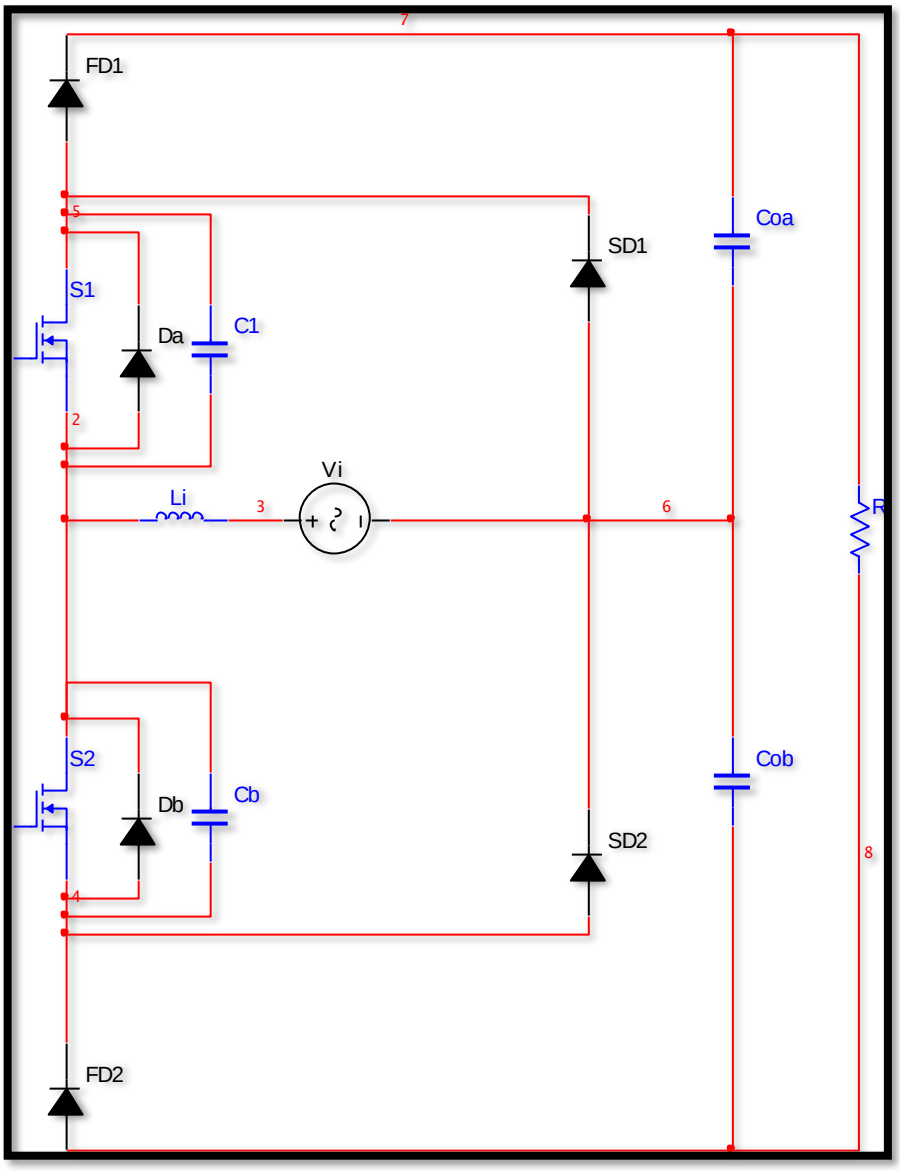

Fig.2.1. Proposed converter

The proposed topology needs only one inductor and their device utilization factor is very high. In this circuit two slow diodes (S_{D1} & S_{D2}) can be used as rectifier diode as

well as voltage clamping diode simultaneously. By this nature voltage clamping can be achieved. Two output capacitors (C_{0a} & C_{0b}) are also connected in the circuit to clamp the line output to reduce the conduction mode noise. And by this the total output voltage becomes high due to the series output structure. And it can be used for inverter or uninterrupted power supplies. In this circuit two MOSFET are used as switch (S_2 & S_2) this two MOSFET are connected with two intrinsic diode (D_{i1} & D_{i2}) and two junction capacitors (J_{c1} & J_{c2}), F_{D1} & F_{D2} are the fast diode & L_i is the input inductors connected to the MOSFETs , R_0 is the load resistance $V_i(t)$ is the line input & V_{0a} & V_{0b} are the output voltages ($V_{0a} = V_{0b} = V_0$).

The proposed converter circuit can be used as two separate boost converter circuit for each output signal during half time cycle. To make circuit simple all the devices are assumed to be ideal. The output capacitor are kept so large so that the voltage in output are remains constant.

2.1 Modes and Stages of the Proposed Converter Circuit:

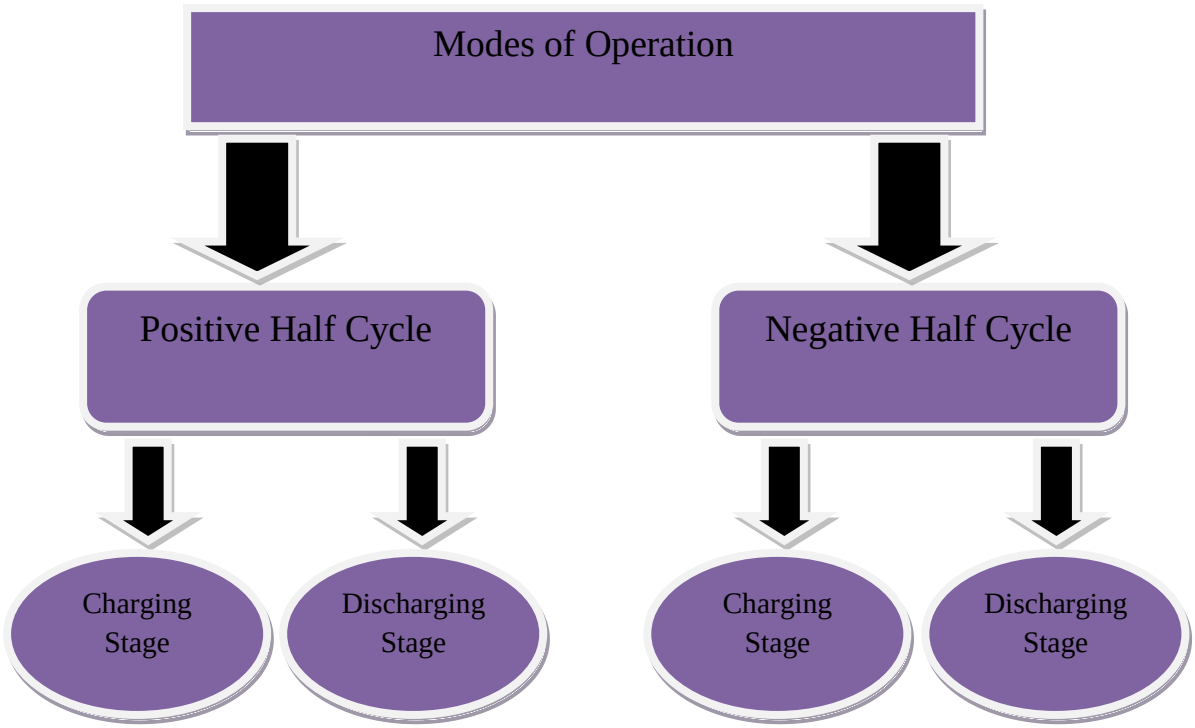

Fig.2.2. modes and stages of operation.

Converter Circuit has Mainly Four Conditions Given Below:

(a). Charging stage in the positive half cycle.

(b). Discharging stage in the positive half cycle.

(c). Charging stage in negative half cycle.

(d). Discharging stage in negative half cycle.

The description of all four conditions will be describe in the next page in which all four circuits with their description will be given.

2.2.1. Charging Stage of Positive Half Cycle:

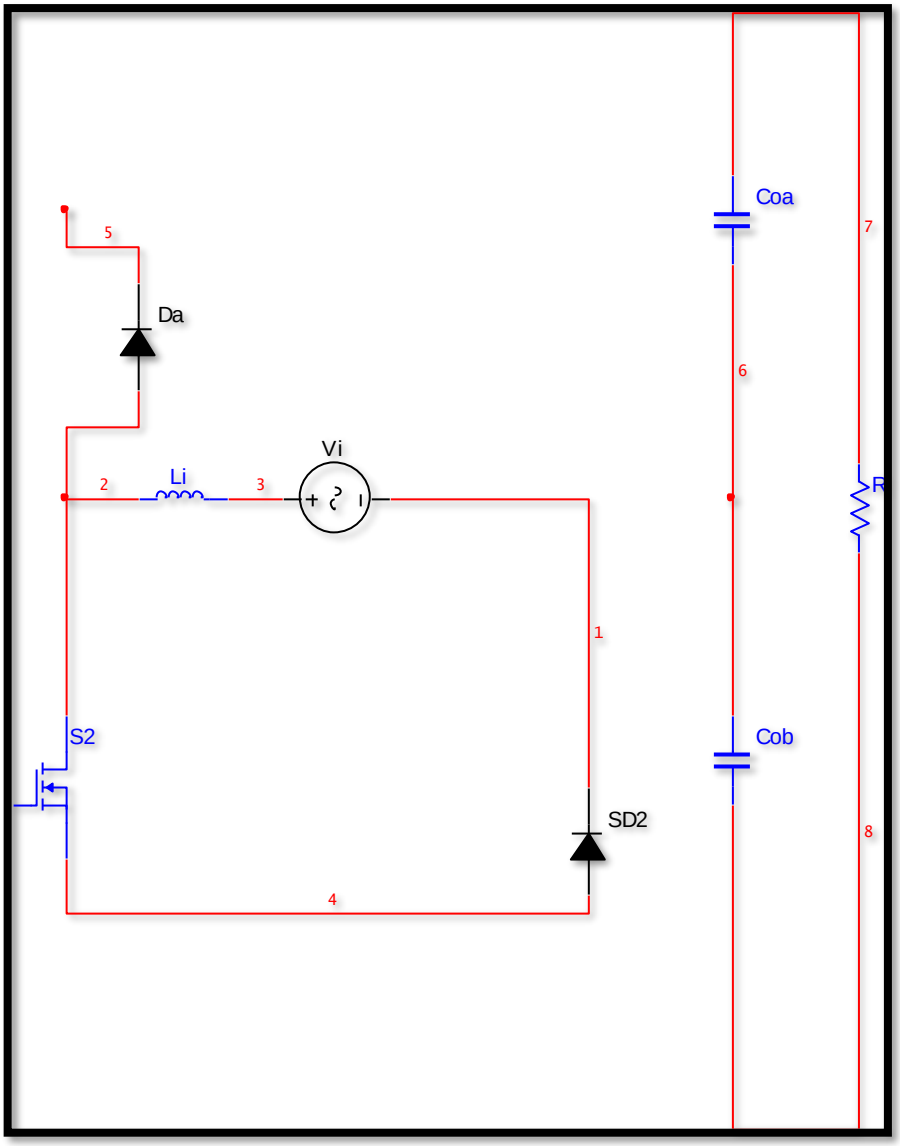

Fig.2.3. Charging stage of positive half cycle

During charging stage of positive half cycle the circuit works between t_a to t_b switch s_2 turns on at t_a the current is commutated from F_{D1} and D_a to S_2 and S_{d2} . as F_{D1} & D_a are connected in series and reverse recovery of F_{D1} and D_a are dominated by F_{D1} (fast diode) and hence the F_{D1} blocks the whole voltage of reverse recovery and D_a is still forward biased without current. When S_2 is fully on then the voltage across the F_{D1} is clamped to V_{0a} by D_a , S_2 and S_{D2} .

During the stage the current of inductor is charged up by the input voltage $V_i(t)$ & it increases linearly . the capacitor C_{0a} and C_{0b} delivers the power to load in series . D_a is forward biased and S_2 & S_{D2} are in on state so , the voltage across F_{D1} , S_{D1} & F_{D2} are V_{0a} , 0 & V_{0b} respectively this stage stops when the switch S_2 turns of at t_a.

In this operation we assume the MOSFET as a switch hence its abbreviation is assumed to be S_1 and S_2 because in the whole operation the MOSFET works as a semiconductor power electronics switches. And two diodes are working as rectifier diode and voltage clamping diode.

Now in the next page we will discuss about the discharging stage of positive half cycle.

2.2.2. Discharging Stage of Positive Half Cycle:

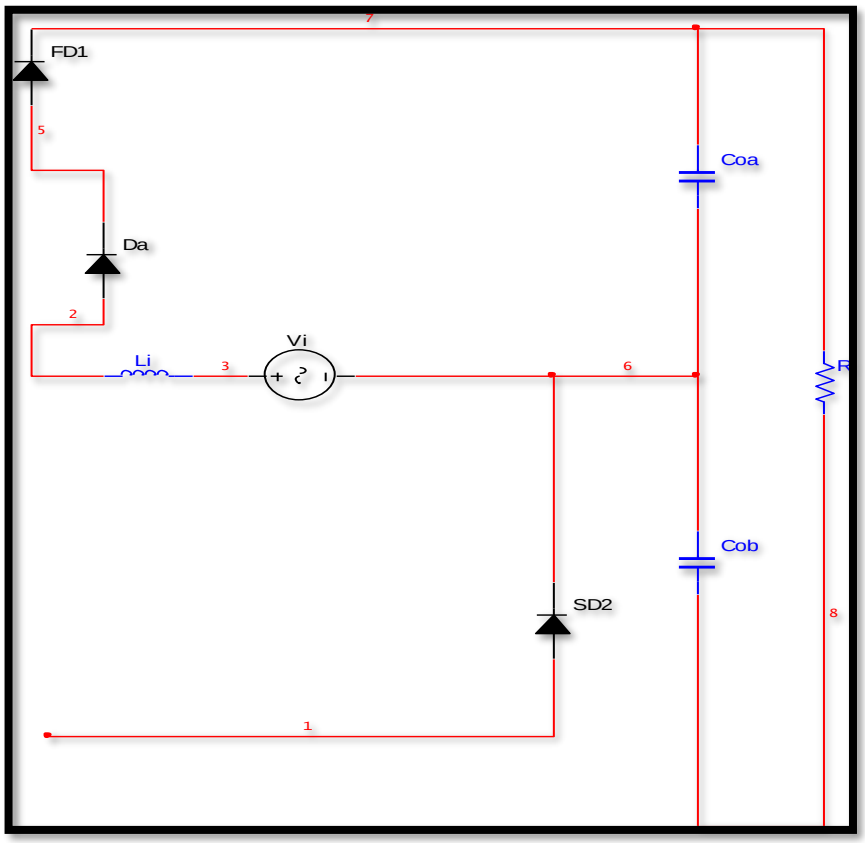

Fig.2.4. Discharging stage of positive half cycle.

During discharging stage t_b to t_c , at t_b s_2 turns the current is shifted from S_2 to & S_{D2} to F_{D1} and D_a . S_2 and S_{D2} are in series & S_2 is a MOSFET there is no issue of there is no issue of reverse recovery theoretically for the slow diode. In next section it will be further explained as the result when the S_2 is fully off , S_{D2} is still on without current & the voltage across the S_2 is clamped to V_{0a} by S_{D2} , D_a & F_{D1} .

In this stage the inductor L_i current is discharged & also decreases linearly. The capacitor C_{0a} is charged up and the capacitor C_{0b} is still delivers the power to load since S_{D2} is forward biased and F_{D1} and D_a are in the ON state , so that the voltage across S_{D1}, s_2 and F_{D2} are $V_{0a,}$ V_{0a}, & V_{0b} respectively.

This mode ends when the switch S_2 turns ON at t_c again.

In the negative half cycle the procedure is of the stages are same whose diagram of the circuit and their description are given which is similar to the positive half cycle and only the working components reverse their working cycle but the overall working is same as that of the positive half cycle.

2.2.3 Charging Stage of Negative Half Cycle:

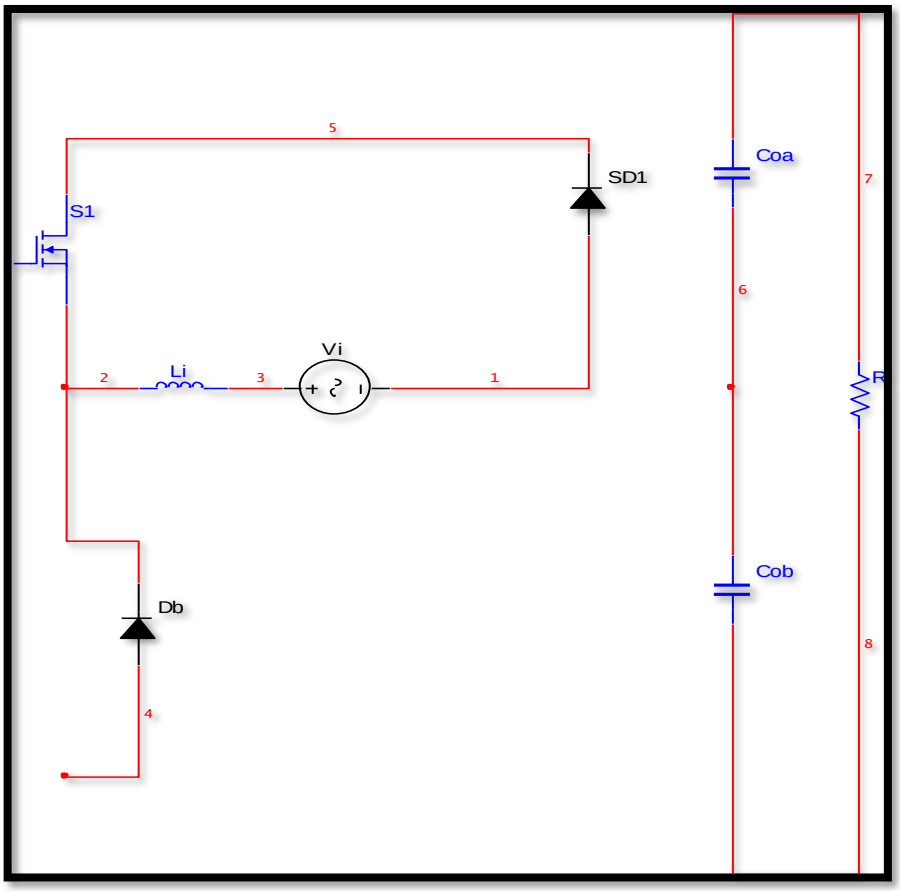

Fig.2.5 Charging stage of negative half cycle.

During discharging stage the period between t_d to t_e. S_1 turn on at t_d . the current commutated from F_{D2} and D_b are connected in series the reverse recovery of F_{D2} and D_b are dominated by the fast diode F_{D2} . thus F_{D1} blocks the whole reverse voltage & D_b is still forward biased without current. When S_1 is fully ON the voltage across F_{D2} is clamped to V_{0b} by D_b, S_1 & S_{D1} .

During this stage the inductor (L_i) current charged by input voltage $V_i(t)$ and increases linearly . the capacitor C_{0a} and C_{0b} delivers the power to the load in series. D_b is forward biased and S_1 and S_{D1} are in ON state. So, the voltage across F_{D2} , s_{D2} and F_{D1} are V_{0b}, 0 and V_{0a} respectively .this stage stops working when the switch S_1 turns of at t_e.

These are the descriptive explanation of the charging mode in the negative half cycle in which the inductor of the power factor correction circuit based on the boost converter is working in the charging mode. And the discharging mode will be discussed just next after this charging mode.

2.2.4. Discharging Mode of Negative Half Cycle:

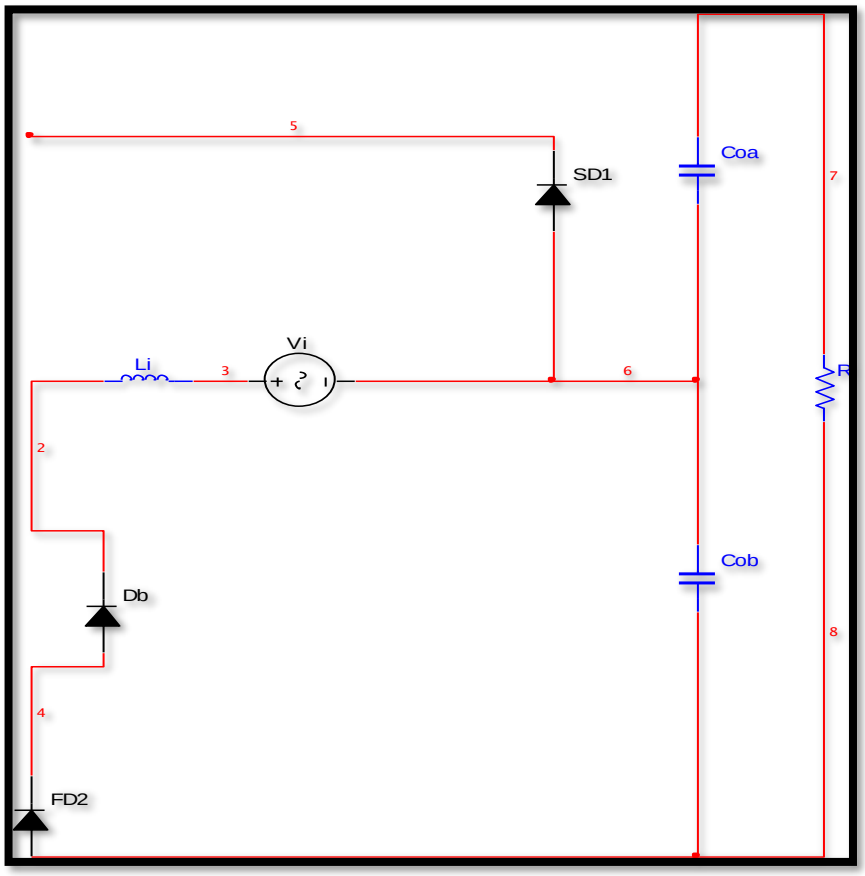

Fig.2.6 Discharging stage of negative half cycle.

During discharging stage if negative half cycle the period is from t_e to t_f . at t_e S_1 turns off . The current is shifted from S_1 and S_{D1} to F_{D2} and D_b. As S_1 and S_{D1} to F_{D2} & D_b. As S_1 and S_{D1} are in series & s_2 is a MOSFET.

There is no reverse recovery voltage for slow diode theoretically. It will explain in the next part. as a result when S_1 is fully off , S_{D1} is still ON with no current & the voltage across the S_1 clamped to V_{0b} by D_{D1} , D_b & F_{D2}. In this stage the inductor L_i current is

discharged and decreases linearly. The capacitor C_{0b} is charged up and the capacitor C_{0a} still delivers power to the load. S_{D1} is forward biased and F_{D2} and D_b are in the ON state. So the voltage across S_{D2} , S_1 and F_{D1} are V_{0b} , V_{0b} , and V_{0a} this mode ends when S_1 turns ON at t_f again.

2.3 Switching Transient during Reverse Recovery of Diode:

As description given above, the slow diode S_{D2} and MOSFET body diode D_a conducts the current during the discharging and charging stage. We all know that the performance of the reverse recovery of the body diode of the MOSFET and also its slow diode is much poor due to the very large reverse recovery charge. And that's why their characteristics of reverse recovery should be considered carefully. Because the reverse recovery characteristics of the semiconductor can introduces losses and by hence decreases the circuit efficiency.

2.4 Reverse Recovery of the MOSFET Body Diode:

During the stage of discharging body diode of MOSFET D_a conducts current with F_{D1} (fast diode) at the end of discharging stage, when S_2 turns ON , the current through the two diode (such as D_a, F_{D1}), is commutated to MOSFET S_2.

When both diodes are in series mode, then the charge or the current through the diodes are same. And their process of commutation is described below briefly.

At t_a switch S_2(here in this report MOSFET is treated as switch so is written as switch) turns ON . the current through F_{D1} and D_a decreases. The slew rate of current is limited by the circuit parasitic inductance and switch turn ON speed.

At t_b, the current through F_{D1} & D_a reaches zero. The reverse recovery starts of both the series diode. The reverse recovery charge of D_a is much larger than the fast diode F_{D1}.

At t_2 the reverse recovery charger of fast diode F_{D1} is totally removed and F_{D1} begins starts to block the reverse voltage. However, the reverse recovery of D_a is not finished till now. And hence it is in on state during (t_c to t_d). V_{0a} the reverse voltage is totally applied to F_{D1} after t_d . the reverse recovery current of D_a will not happen after t_d, there is no reverse voltage applied to D_a its internal extreme charge can only be separate by interior recombination and it takes fairly long time for a switching cycle , the time is two extended and the MOSFET body diode can be treat as short circuit.

Based on the explanation above, the reverse recovery performance of diodes which in series is conquered by the fast diode and also the slow diode can be shortened.

2.5 Reverse Recovery of the Slow Diode:

During the period of charging the slow diode S_{D2} and switch S_2 conducts the current. When the charging stage ends S_2 turns off and the current through S_2 and S_{D2} will commutate to D_a and F_D .

As the slow diode has very deprived reverse recovery characteristics.

Its reverse recovery characteristics must be carefully measured at the switching transient. As S_2 and S_{D2} are in series , the current through them is same too.

At t_a , S_2 turns off. The D to S voltage V_{DS} of S_2 increases. When V_{DS} reaches half the output voltage V at t_b . the diode D_a and F_{D1} are forward biased and the current commutation starts. The current through S_2 and S_{D2} starts to decreases. At instant when the current reaches "0" at t_c . S_2 is fully off . since the MOSFET is majority device there is complete no reverse recovery current. Although excessive carriers remain in slow diode S_{D2}, reverse recovery current is absent in it, the switch S_2 blocks the entire reverse voltage. There is no negative voltage applied to S_{D2}. The extreme chargers in SD2 keep it in on state. The minority in S_{D2} can only be take away by internal recombination, Which requires quite a long time.

And hence in switching cycle, S_{D2} can be treat as short circuit and therefore nature voltage clamp is achieved.

Based on the above analysis the slow diode's reverse recovery in series with a MOSFET is dominated. And there is no any reverse recovery current is present by use of slow diode.

The above description is all about the working of the proposed converter circuit of power factor correction using soft switching. In next chapter we will discuss about the design consideration and the working device description.

CHAPTER 3

EVALUATION OF PERFORMANCE

In this chapter we will discuss the performance of the proposed converter in detail

3.1 Attached Slow Diodes:

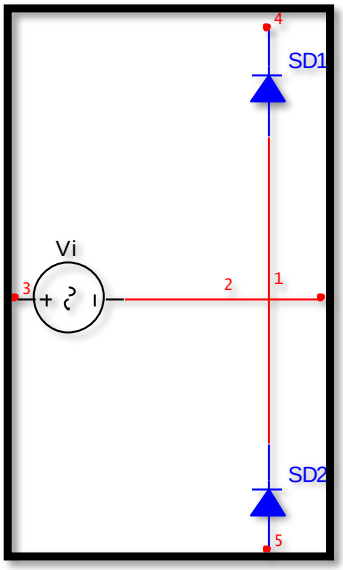

Fig.3.1. Showing the attached slow diodes

As discussed in the previous section, between the duration of the positive half-line cycle, the slow diode S_{D2} and the body diode D_a were always in forward biased mode. In the charging stage S_{D2} is used as rectifier in the other hand, in discharging stage body diode D_a is used as rectifier diode.

In the discharging period, when the current (input current) freewheels through the body diode D_a and the fast diode F_{D1} the whole output voltage will be apply across the switch S_2 and the fast diode F_{D2} . The slow diode S_{D2} is at rest (ON) because of its sluggish recovery. And the result is, the slow diode S_{D2} clamps the voltage across the switch S_2 & the fast diode F_{D2} to V_{0a} and V_{0b} respectively. So that the slow diode S_{D2} also plays an important role for the voltage clamping diode at same time, there is no any requirement of the extra voltage clamping diode for the proposed converter.

Although the body diode and the slow diode operate at high frequency, there is no problem of reverse recovery due to the dominated switching behaviour by the MOSFET or the fast diode as explained above.

3.2 The Characteristics of Voltage Clamping Property:

In the three level converters, the voltage clamping characteristics is extremely important. Or else the entire output voltage will affect across devices. And the result, high voltage rating devices are necessary, which will raise the cost of the circuit. The voltage clamping presentation is quite dissimilar in different topologies.

As explained previously the innovative single inductor three level bridgeless power factor corrections suffer from high voltage stress. As shown in the figure. The described circuit diagram is given below in which the other explanations of the proposed circuit converter circuit is drawing in detail and the working descriptions will also discussed after the given figure below the given figure below is of the existing topologies. And its modified circuit with slow diode will also be discussed after the figure and explanations of the proposed topology.

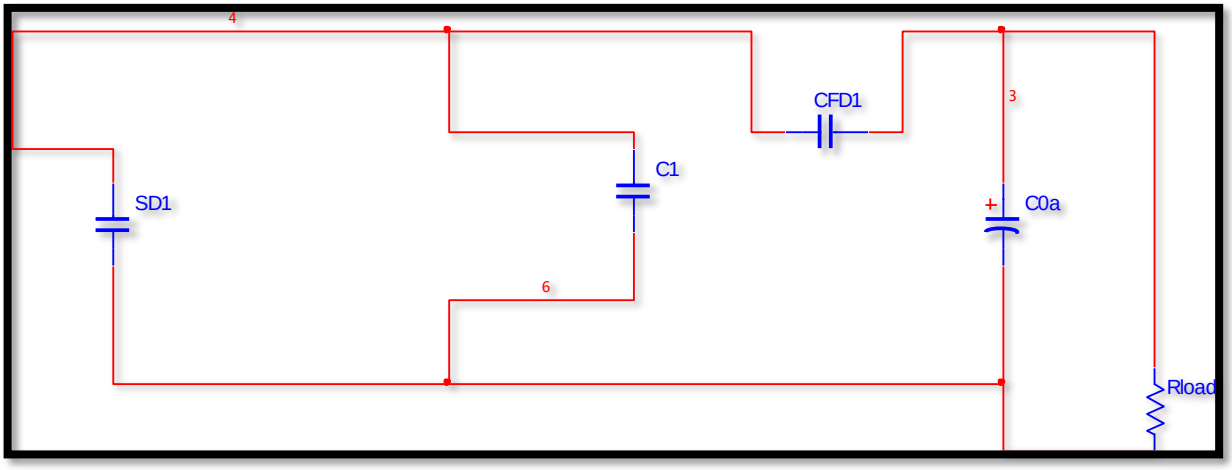

Fig.3.2. Existing topology.

When S_2 operates in pulse width modulation (PWM) mode, point 1 will be connected to point 2 or –V (negative output voltage). Consequently the electric potential of point 1 is pulsating with very high frequency. The Input inductor and line input can be removed by an alike very high-frequency rectangle voltage source with the amplitude of –V. As result the process in the active set circuit will very much affect the voltage distribution in the stopped one because of the parasitic capacitance being unlike. The voltage stresses of device may be doubled,

E.g. the voltage across S_{D1}, and high voltage rate devices are necessary, which may raise the conduction loss.

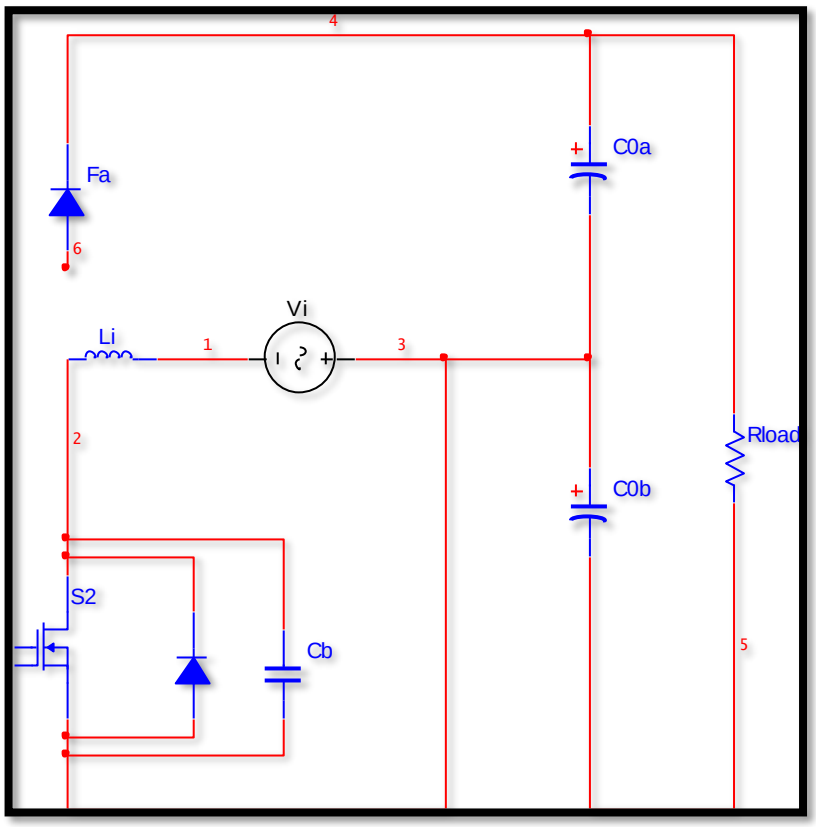

Fig.3.3. Proposed topology with slow diode.

In proposed converter shown in above figure, the earlier voltage clamping issue is eliminated. As shown in the above figure during the positive half cycle, the intrinsic diode D_a and the slow diode S_{D2} can be treated as summarized. The voltage across low down side fast diode F_{D2} is clamped to V_{02}. Only point K is pulsating as a result of pulse width modulation (PWM) operation of S_2. The voltage stress of all the semi conductor devices are 1/2 of the whole output voltage. The voltage clamping is perfect & no extra clamping diodes are necessary. The voltage clamping performance of the projected topology is the best one between these three level boost bridgeless power factor correction rectifiers.

3.3 Enhanced Properties of Proposed Converter:

(a). Utilization factor of device is very high.

In the proposed converter, it has the highest device operation factor, double output DC bus with only nine power components. In fact it can be proved that the amount of components cannot be made smaller. First each set boost circuit requires a MOSFET with a fast diode. Secondly, dissimilar in 3-phase application, which is essential to achieved, there must be two rectifier diodes to disconnect the positive half cycle and the negative half cycle in 1-phase applications, which is necessary to achieve bridgeless in

topology. Finally, two outputs DC buses need two output capacitors. Though there is no prohibition on the input inductor's number & the input inductor is joint in proposed converter.

So the total number of semi conductor components in a boost power factor correction rectifier with the dual-output DC buses is at least nine in 1-phase applications.

(b). Low conduction losses.

In the proposed converter there were only a slow diode with a MOSFET built-in diode on the discharging path, and only MOSFET built-in diode with a fast diode on the discharging path. And hence the losses of conduction are low in the proposed converter. The MOSFET built-in diode can also be extremely low. It will conduct current very easily with the drop of the forward voltage of the built in diode of the MOSFET can also be very low little.

It will conduct current efficiently with drop of the forward voltage around 1V as a result of the insertion of high attention of minority careers into the drift area of the MOSFET. Also the MOSFET can always be on to further decrease the loss of conduction.

(c). Low conduction mode (CM) noise.

In the proposed converter the output DC bus are coupled to the line through the big output capacitors. And hence the output potential is very secure and CM noise is theoretically low.

These all are the explanations about the performance of the proposed converter, in the next chapter we will discuss about the design considerations.

CHAPTER 4

DESIGN CONSIDERATION

The proposed converter can be treated as continues current mode (CCM), discontinuous current mode (DCM) and current resonance mode (CRM), and the operation is similar to the traditional single switch converter. The design method of conventional single switch boost power factor correction can be applied for the proposed converter. Due to the series output structure, the output capacitance design is a little different, which is explained below.

The output capacitor is charged up throughout half cycle and discharged by the load current in the left over half cycle. so the charge current I_{chg} and the discharged current I_{dischd} through each capacitor in a line cycle are given below.

$$I_{CHD} = I_0 - 2I_0 \cos(2\pi f_L t) \quad \text{(a)}$$

$$I_{dischd} = -I_0 \quad \text{(b)}$$

Where f_L is the line frequency and I_0 is the DC output current.

Based on the above equation the RMS current for the each capacitors are given in the next equation which is double then that in the conventional boost power factor correction converter. It is reasonable due to the series output structure.

$$I_{CRMS} = \sqrt{2}I_0 \quad \text{(c)}$$

Based on the capacitor discharge and charge current given in the equation (a), the voltage ripple for the output capacitor C_0 can be introduce as

$$\Delta V_C = I_0 \frac{1}{2\pi f_{LC_0}} \left(\frac{\sqrt{3}}{2} + \frac{5\pi}{6}\right) \quad \text{(d)}$$

Peak to peak output ripple voltage is the addition of the two capacitors (voltage ripple) which is given in the next equation it is double than that in a traditional boost PFC converter

$$V_r = 2I_0 \frac{1}{2\pi f_{LC_0}} \quad \text{(e)}$$

The output capacitance can be designed based on the required voltage ripple given in equation (e) and its RMS current is given in (c).

Now we will discuss in detail on the design consideration of power electronics devices I.e MOSFET, capacitors, diodes, resistor, inductor and their properties with their specification by the making of different table for the different categories of these power

electronics devices in this tables we will discuss their different properties and their ratings in detail.

4.1 Design Consideration of Power Electronics Devices (Switches and Diodes):

4.1.1 Selection of Switches.

Switch is the key of any circuit and its selection for the working of the circuit is very essential on giving the attention on the switching frequency (speed of ON-OFF) , efficiency and their working operations so their selection for decreases the voltage and current stress , increasing the efficiency and speeding up the switching frequency and decreases the conduction losses , the soft switching is designed for the precisions of CCM, DCM & CRM.

These switches and devices are MOSFETs, diodes, capacitors, inductors etc and Now we will discuss in detail on the design consideration of power electronics devices I.e MOSFET, capacitors, diodes, resistor, inductor and their properties with their specification by the making of different table for the different categories of these power electronics devices in this tables we will discuss their different properties and their ratings in detail.

4.1.2 MOSFET.

Electrical Characteristics, (at *T*j = 25 °C, unless otherwise specified)

Table.4.1. shows the electrical characteristics of MOSFET [13]

Symbol	**Parameter**	**Value**	**Unit**
V_{GS}	Gate to source voltage	±20	V
I_{GSS}	Gate source leakage current	100	nA
$R_{DS(ON)}$	Drain- source ON state resistance	0.06 to 0.07	**Ω**

The above is the characteristics of the switching MOSFET which is used in the proposed topology as S_1 and S_2 . All these data is collected in the name of SPW47N60C3 which is a slandered MOSFET these all data is collected from the reference [13] .

And this component is of very high frequency and very high precisions which is used in the circuit very easily. This model is the best suitable for the proposed circuit.

4.1.3 DIODES:

Selection of diodes

The selection of the diodes in the proposed circuit is very much specified there are three different types of diodes are given and these diodes are fast diode, slow diode and the MOSFET body diode, whose description will discussed in the next tables.

Slow diode

Slow diodes are those diodes whose switching frequency is slow and is use for the reduction of the losses in the circuit. i.e S_{D1} and $S_{D2.}$ It has very slow reverse recovery characteristics and is used for the voltage clamping in the converter.

Fast diode

Fast diodes are that diode whose operating frequency is very high and this diode is used in the converter circuit for fast recovery because this diode has very fast reverse recovery characteristics.

(a) Slow diode

ELECTRICAL CHARACTERISTICS

Table.4.2. The electrical characteristics of slow diode [14].

Symbol	**Parameter**	**value**	**Unit**
VGS(th)	Gate Threshold Voltage	1.2	V
RDS(on)	Static Drain-source On Resistance	0.25	**Ω**
ID(on)	On State Drain Current	25	A

The above data of table no.3.2 is related to the slow diode and the data is collected from the reference [14] this slow diode is of the type of KBPC3510 which is very much suitable for the proposed circuit or we can say that this diode is the best suitable for the circuit. Its accuracy and precision are very good and loss of the electrical power is also very much less.

Now after this table we will discuss about the electrical parameter detail of the fast diode in detail.

(b)Fast diode

ELECTRICAL CHARACTERISTICS

Table.4.3. The electrical characteristics of fast diode [15]

Symbol	**Parameter**	**value**	**Unit**
VGS(th)	Gate Threshold Voltage	2.1	V
RDS(on)	Static Drain-source On Resistance	0.29	Ω
ID(on)	On State Drain Current	12	A

The above data given in the table no. 3.3 related to the slow diode and the data is collected from the reference [15]. These all the detail is related to the model IDH12SG60C. Which is very much suitable for the proposed circuit or we can say that this diode is the best suitable for the circuit. Its accuracy and precision are very good and loss of the electrical power is also very much less.

4.2. Soft Switching of the Proposed Topology.

though this three-level boost converter already has little bit switching losses than the traditional boost converter, soft switching method is still appreciated for high power, high voltage & high switching frequency applications.

Directly relate the zero voltage transition method, the zero voltage transition three level boost converters by addition of two slow diodes & the two resonant networks.

Mainly the top resonant network achieves the zero voltage switching (ZVS) for the top switch S_1 and the lower resonant network for the bottom switch S_2 . as the turn on action on the two main switches are interleaved the supplementary networks are also operating alternately.

The supplementary switch driving signal is applied a little period before the turn on of the equivalent main switch so that a current build up in the resonant inductor.

When the resonant inductor current reach the boost inductor current, resonance occurs among the resonant inductor & the resonant capacitor, which is the junction capacitor

of the main switch jointly with external capacitor, if any. The anti-parallel diode of the main switch will conduct & and this resonance will discharge the resonance capacitor. And by this the zero voltage switching state is achieved. It is noted that the energy in the upper resonant inductor is released to the upper output capacitor & the energy in lower resonant inductor is released to lower output capacitor, respectively, which ensures the voltage of the output capacitor.

All the supplementary device are also rated at half of the output voltage, which has not as much of conduction and switching losses than the supplementary device in the traditional ZVT boost converter.

CHAPTER 5

SIMULATION AND ITS RESULT

In this chapter the proposed topology is simulated and the explained result of simulation is elaborated. The simulation is done in the SIMULINK, a part of the software called MATLAB.

5.1. MATLAB Software:

MATLAB is a software whose name is comes from the two different words, MATRIX & LABORATORY, MAT is comes from the word MATRIX & LAB is comes from the word LABORATORY.

It is a very useful and versatile software which is invented newly (it is not a very old soft ware.), this software has different types mathematical operators which solve the different large & complex problems by its inbuilt formula and mathematical operators.

5.1.1. Simulation Software:

Simulation is the other part of the MATLAB software in which construction and operation of the different types of large and complex circuit by joining different types of components and source which is inbuilt in this SIMULINK part. Use of the SIMULINK software has different advantages given below.

Advantage of the use of the SIMULINK software in construction of the circuit.

(1).Very large amount of components is available.

(2). Any component to the related circuit are available on the single click.

(3). Different types of related wave form will generate.

(4). Accuracy and precision in the working.

(5). Perfect designing and output is obtained without any chance of mistake.

This all the description about the MATLAB SIMULINK and their advantage and working now we will discuss on the simulated circuit, their diagram, and output waveforms.

5.2.Simulation and Experimental Result.

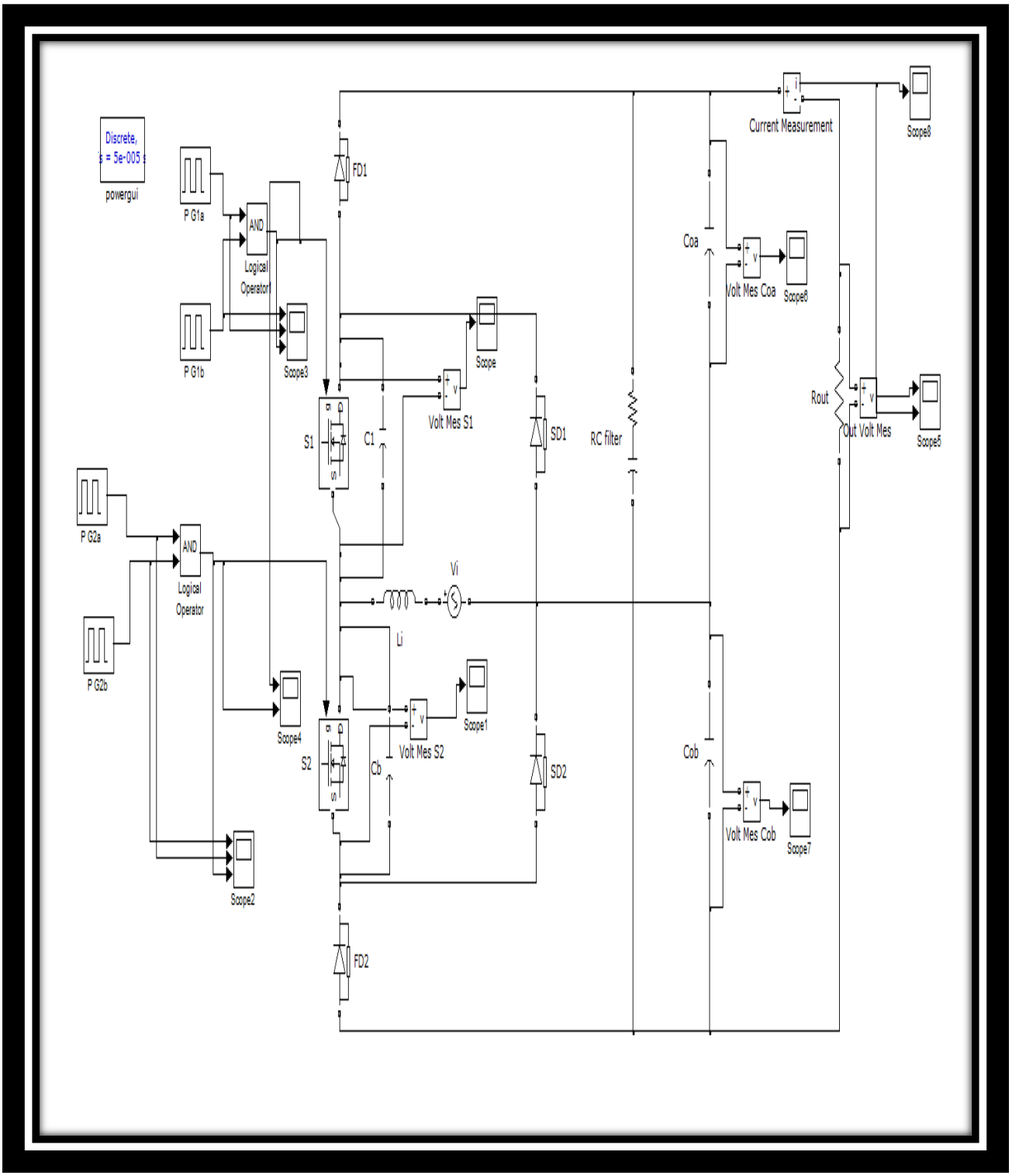

Fig.5.1.Equivalent circuit of proposed topology in SIMULINK

Figure 5.1 is the equivalent simulated proposed topology, in which two fast diodes (F_{D1} and F_{D2}) and two slow diodes (S_{D1} and S_{D2}) are connected to the circuit because of their different work on different timings. The reverse recovery of the slow diode is very slow

and the properties of voltage clamping makes it important in the circuit where as the fast diode has very high reverse recovery characteristics, two MOSFET is used in the circuit as the main switch naming S_1 and S_2. Capacitors are used for delivering the power to the load in series. Inductor is used in the circuit for charging and discharging purposes.

All above component is simulated in the manner discussed previously and the output of the simulated circuit will obtain. All the components are of the same parameter which is discussed in the different tables of chapter no. 4 in which the detailed description of the given component is discussed.

Now we will discuss on the different parameter of the component used in the simulated circuit.

Table5.1.Components and their parameter for simulate the proposed circuit.

SYMBOL	**PARAMETER**	**SPECIFICATION**
$V_i(t)$	Line input	246v RMS, 796v DC, 1000w, 1.25A
V_{0a}/V_{0b}	DC buses	400VDC ±5%
V	Total output voltage	800VDC
P	Full output power	1000W
$F_{switching}$	Switching frequency	100kHz
S_1,S_2	MOSFET	SPW47N60C3
$F_{D1,}F_{D2}$	Fast diode	IDH12S60C
S_{D1},S_{D2}	Slow diode	KBPC3510
L_i	Input inductor	700µH
$C_{0a,}C_{0b}$	Output capacitor	2mF

The table 5.1 is the list of the related components used in the simulation of the proposed circuit. Their specification is also mentioned in that table and these components are listed in that manner in which at the time of joining of the circuit and the simulation of

the circuit there is no any problem of the specification and missing of the necessary component.

5.3 Wave Forms across the Switches.

5.3.1 Input Gate Pulse Waveform of the Switch S_1.

The output wave form of the auxiliary switch is given below which is operating in the positive half cycle.

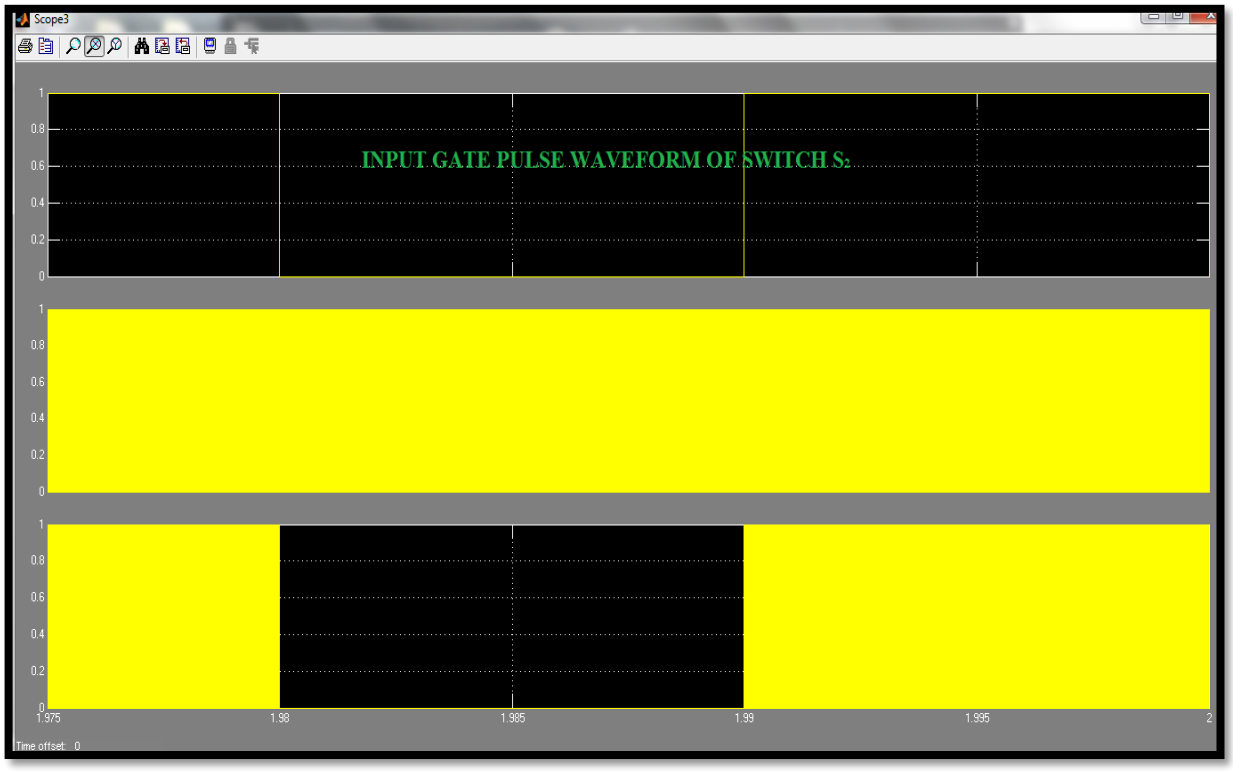

Fig. 5.2.The input gate pulse waveform of the switch S_1.

In case of the first auxiliary switch S_1, it working in the positive half cycle and since it is connected through the AND gate hence it gives the out when both the pulse generator gives the pulse otherwise no output will obtain. Because it operates through the AND gate and the output of the AND gate will obtain in the condition only when both the input is positive or one. Now we will discuss about the output wave form of the second auxiliary switch S_2.

5.3.2 Input Gate Pulse Waveform of the Switch S_2.

Fig.5.3.The input gate pulse waveform of the switch S_2

In case of the second auxiliary switch S_2, it working in the negative half cycle and since it is connected through the AND gate hence it gives the out when both the pulse generator gives the pulse otherwise no output will obtain. Because it operates through the AND gate and the output of the AND gate will obtain in the condition only when both the input is positive or one. And now we will discuss about the combined waveform of two auxiliary switches in the main switch in which the input is given to the main switch from the output of the both auxiliary switches S_1 and S_2 and the output will obtain in the same manner of the auxiliary switch.

5.3.3 Combined Waveform of Pulses Given to the Switches.

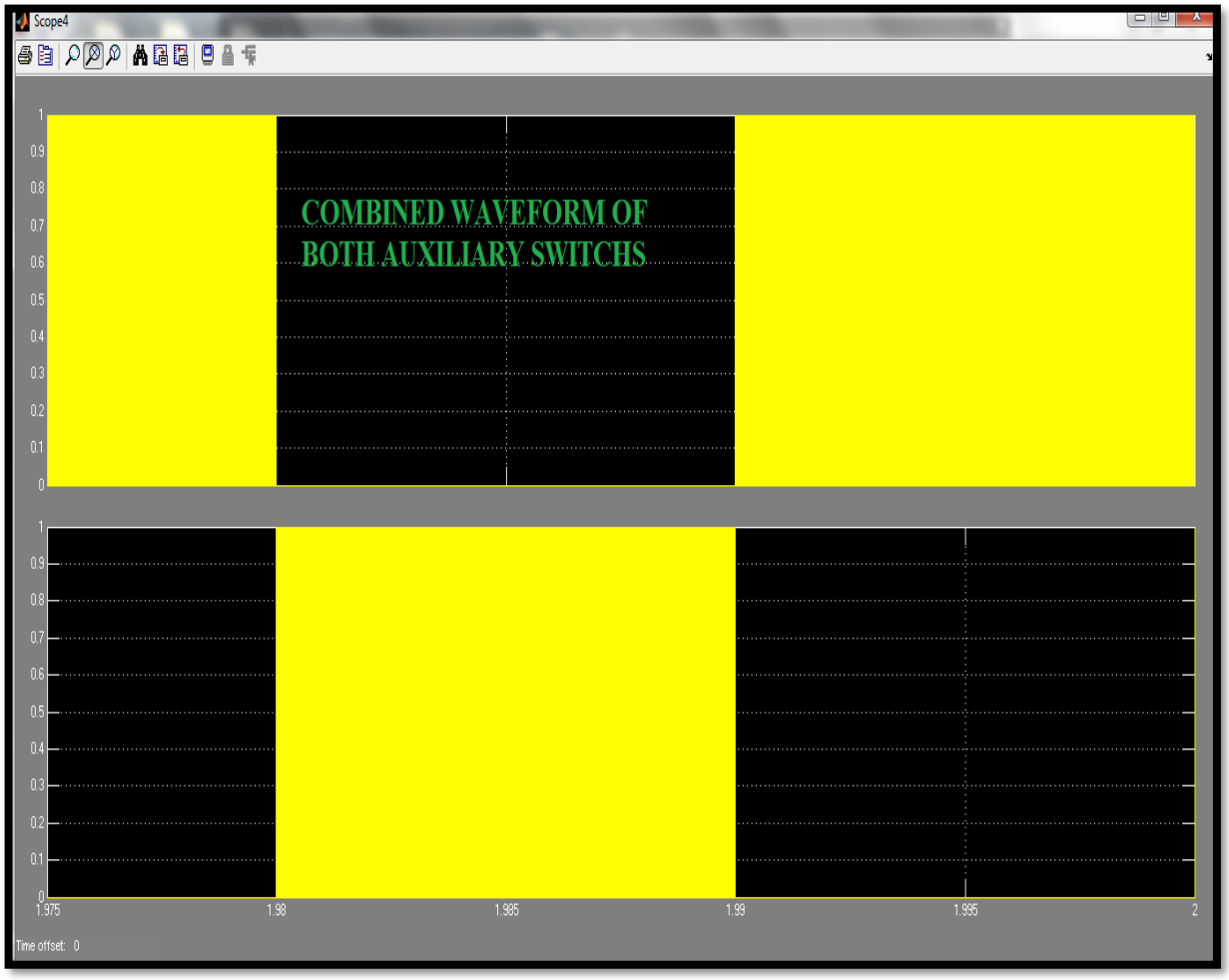

Fig.5.4. Combined waveform of the S_1 and S_2

The above waveform shows the output waveform of the main switch in which the output comes when both the auxiliary switches gives the input to the main switch in the combined form of both the cycle of positive half cycle and negative half cycle .

Since the main switch is also connected to the AND gate and hence it gives the output only in that condition when both the input gives the signal.

Table 5.2 Logic of AND gate

Input 1	**Input 2**	**Output**
1	1	1
1	0	0
0	1	0
0	0	0

5.4. Output Waveforms (Current & Voltage).

Waveform Switch S_1.

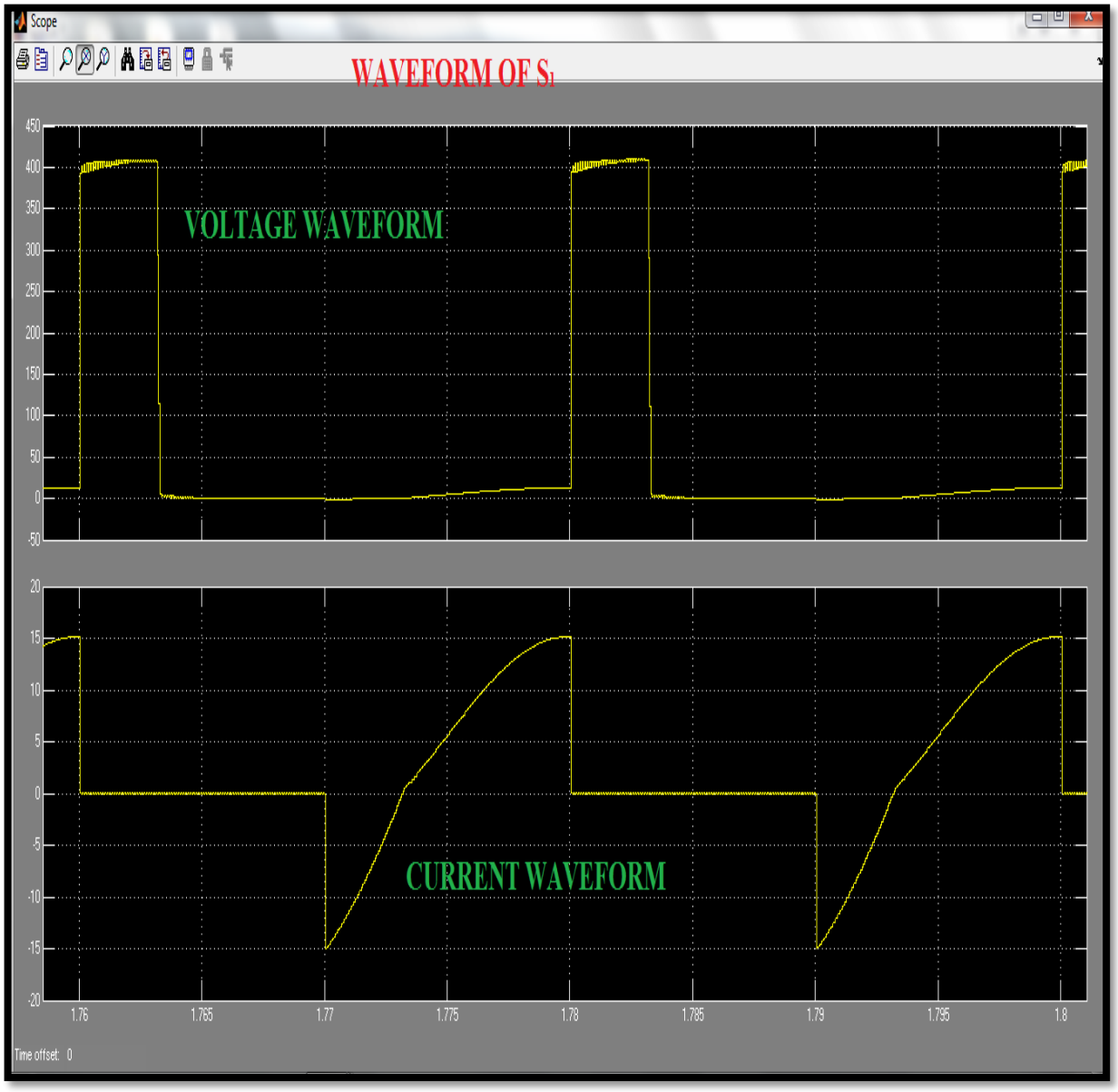

Fig.5.5. Output waveform of switch S_1

In the above figure of output waveform which is obtained from the switch S_1 we have seen that when the current is at the minimum (i.e zero) the value of the voltage is at its maximum

Value and this is the condition satisfy the zero voltage switching (ZVS) where the value of the voltage becomes maximum after when the value of the current becomes zero and after that when the current is going to be increasing the value of the voltage drops drastically and becomes zero , at instant when the current attains its maximum value as

shown in the wave form at the same instant it becomes and the voltage attains its maximum value and this condition satisfy the zero current switching (ZCS).

Waveform of Switch S_2

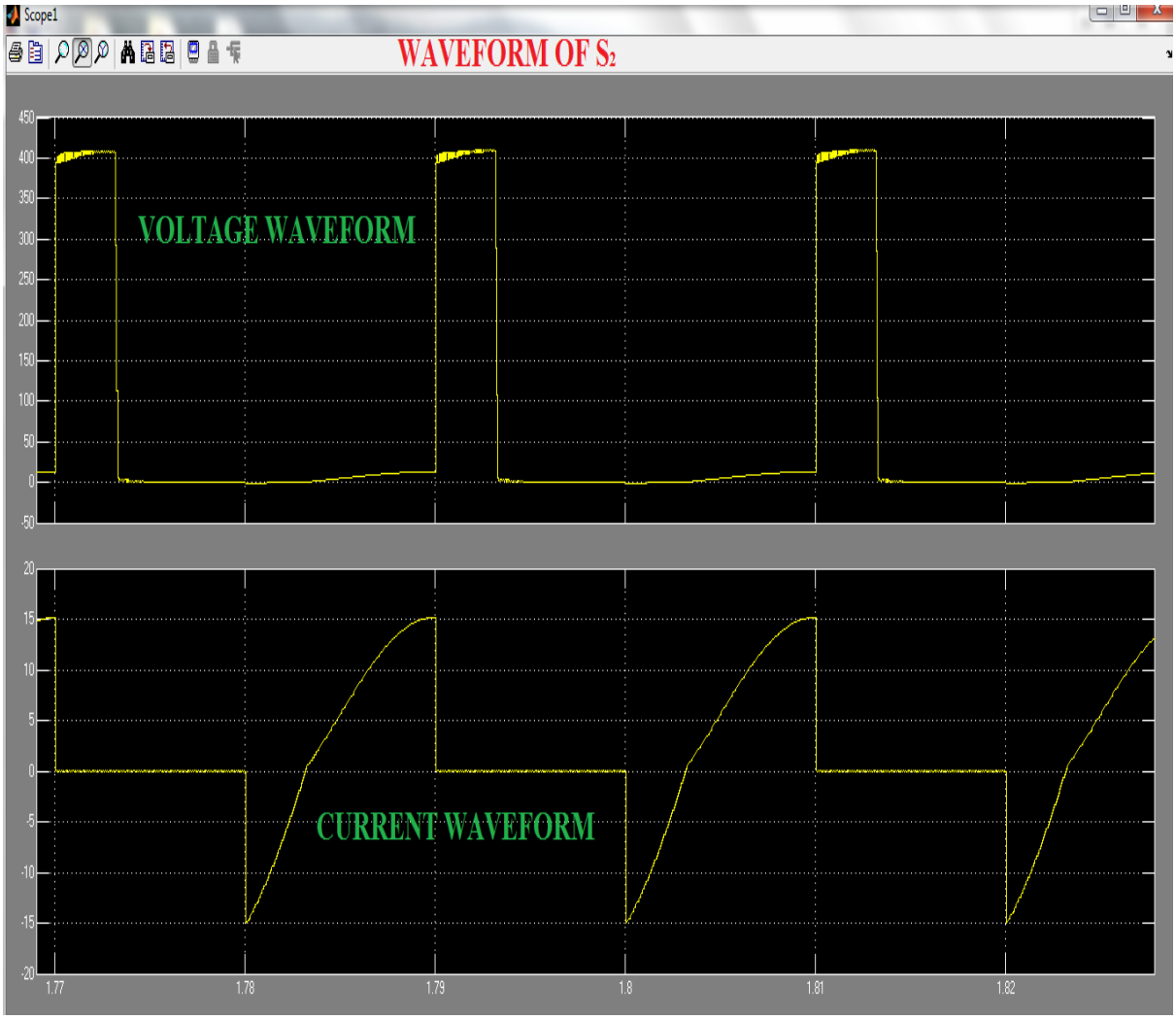

Fig.5.6. Output waveform of switch S_2

The same condition is created in case of the waveform of the switch S_2. Where when the current is at the minimum (i.e zero) the value of the voltage is at its maximum

Value and this is the condition satisfy the zero voltage switching (ZVS) where the value of the voltage becomes maximum after when the value of the current becomes zero and after that when the current is going to be increasing the value of the voltage drops drastically and becomes zero , at instant when the current attains its maximum value as shown in the wave form at the same instant it becomes and the voltage attains its maximum value and this condition satisfy the zero current switching (ZCS).

5.5. Waveform of Output Voltage of Capacitors.

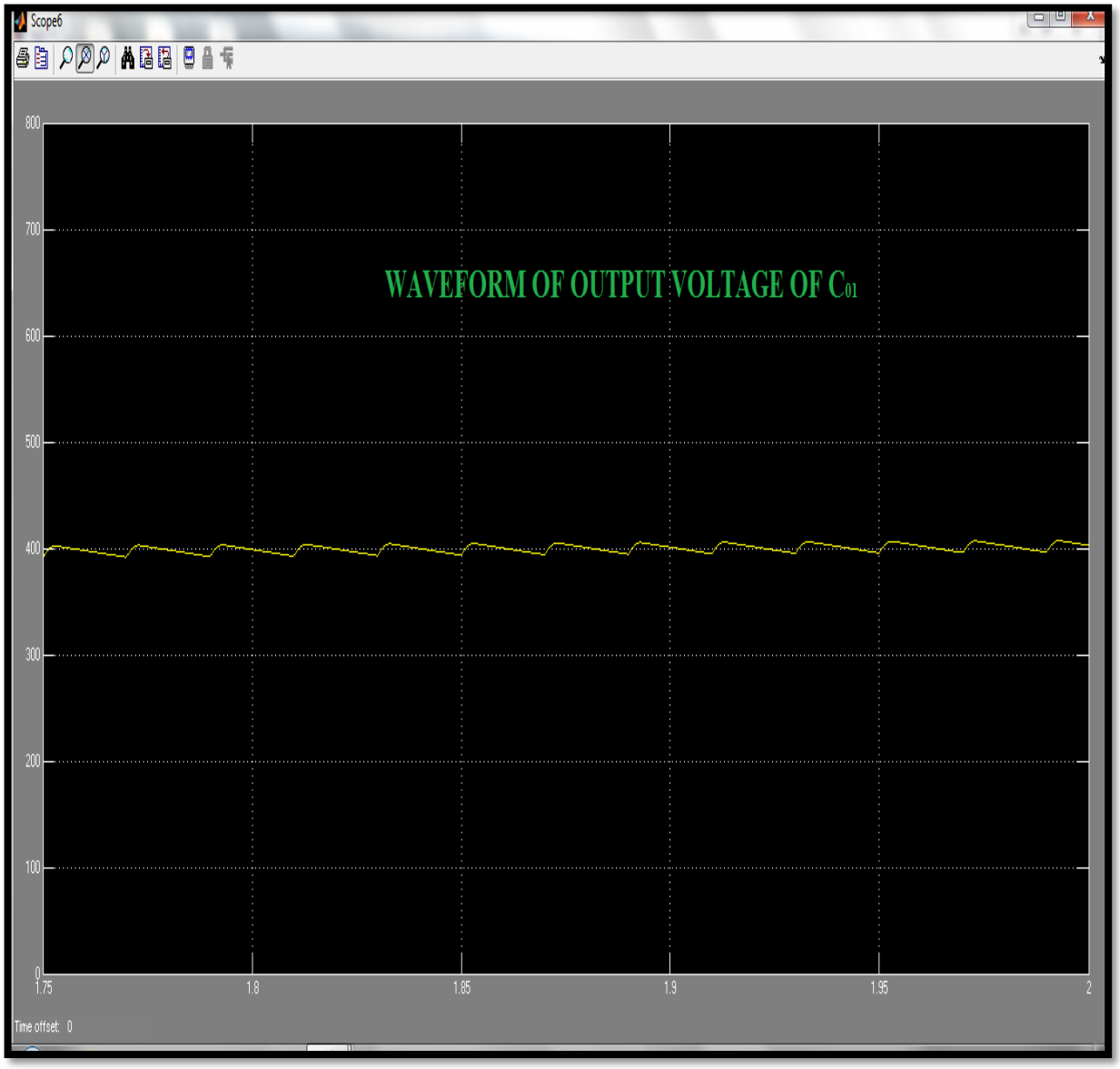

Figure 5.7 Output voltage waveform of capacitor C_{0a}.

The above figure shows the waveform of the output voltage through the first capacitor C_{0a} in which the output of the voltage is achieved at 400V this output voltage is fed from the MOSFET S_1 in which the ZVS and ZCS occurs and this output voltage is fed to the filter (inductor and capacitor) because this output has some ripple or the distortion and the smooth output waveform will obtained with corrected power factor of unity power factor which is a quality power we need.

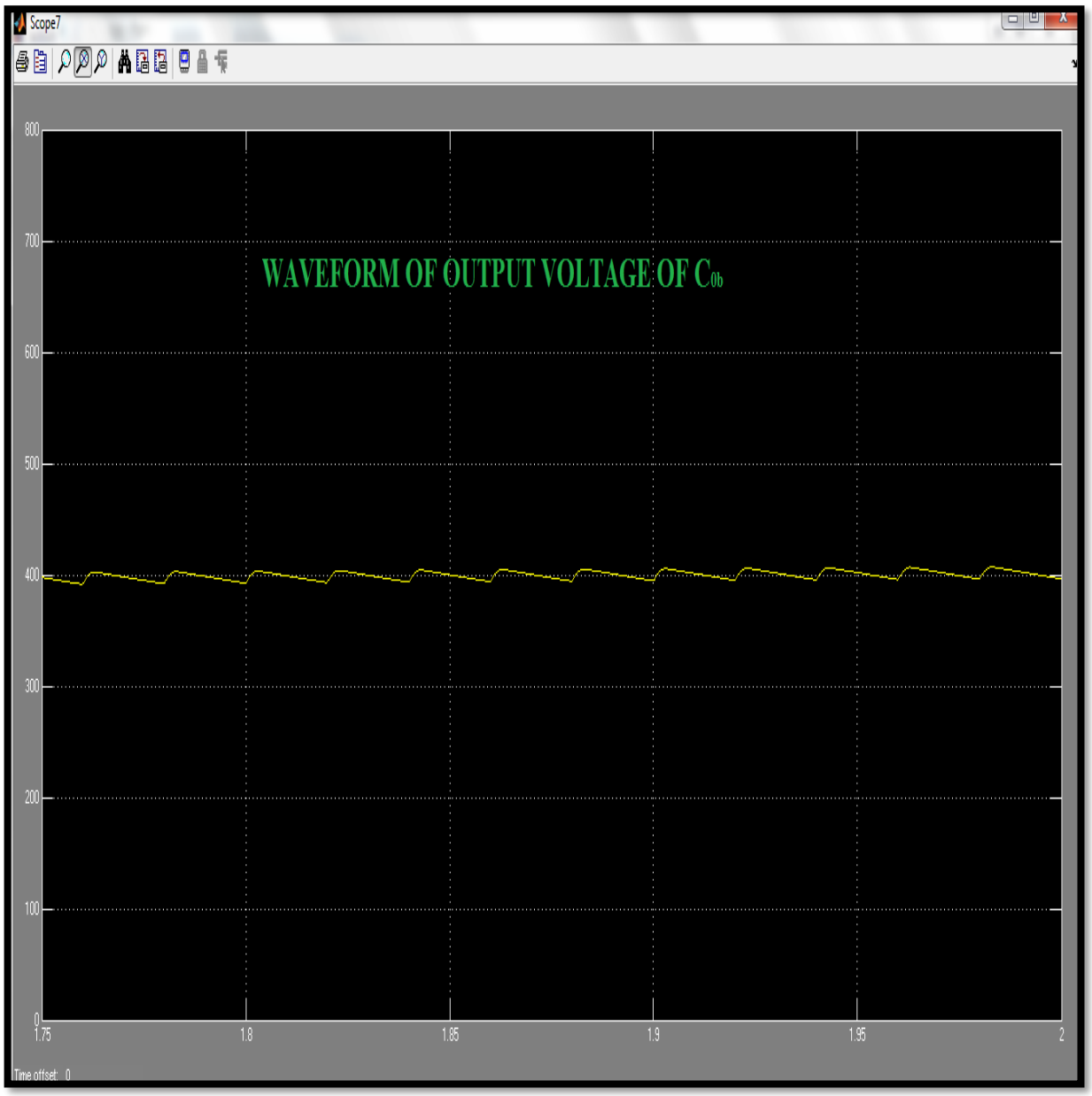

Figure 5.8 Output voltage waveform of capacitor $C_{0b.}$

The same condition occurs in the voltage output waveform of the second capacitor $C_{0b.}$ in which the output of the voltage is achieved at 400V this output voltage is fed from the MOSFET S_2 in which the ZVS and ZCS occurs and this output voltage is fed to the filter (inductor and capacitor) because this output has some ripple or the distortion and the smooth output waveform will obtained with corrected power factor of unity power factor which is a quality power we need.

Now we will discuss on the final load output voltage and current waveform of corrected power factor.

5.6. OUTPUT LOAD WAVEFORM:

5.6.1 Output load waveform of voltage and current with corrected power factor of unity power factor.

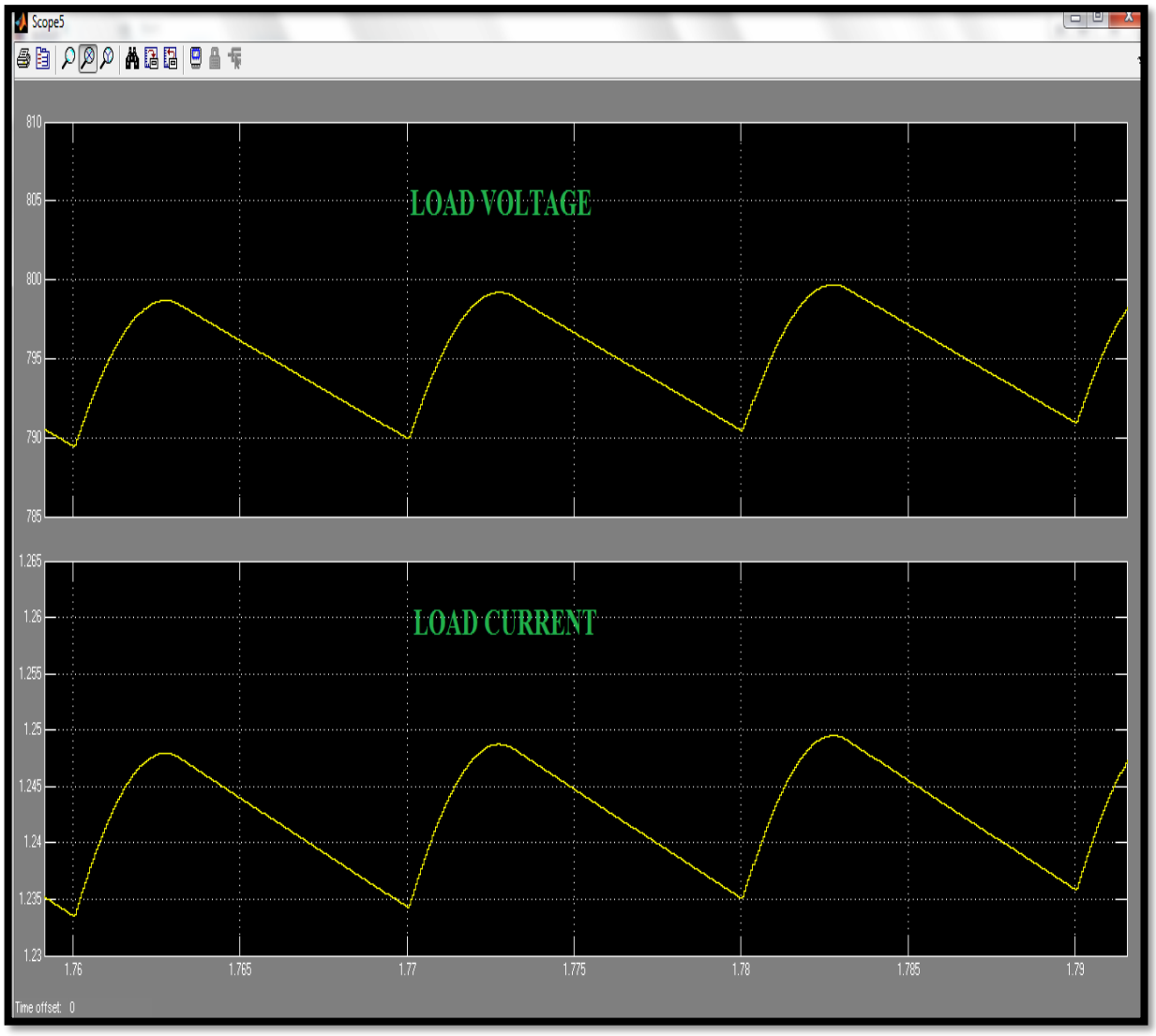

Fig.5.9.Load voltage and current waveform

The waveform of load current and load voltage is shown in this above figure we have seen that when the two voltage signal of 400V each passed through the LC filter then the combined waveform of both the input signal comes from the output capacitor is obtained of 800V and the main thing we have seen is that both the current and the voltage signal are in the same manner., I.e unity power factor or the corrected power factor which gives ideal quality power supply which is good for the uninterrupted power supply or for the battery charging which will give the longer life. And by this we have achieve the main goal of PFC for quality power.

5.7. Comparison of the proposed circuit with ideal supply circuit.

Here we will discuss on the comparison between the proposed circuit and the ideal supply circuit where we will recognise that there is no difference between the output waveform of proposed circuit converter and the output wave form of the ideal supply load waveform, this shows that the circuit which is proposed in this report is very high quality boosting with the maintenance of unity power factor and we can say that boosting of voltage from 373V to 800V DC without losing the quality of power factor means at a voltage range which is almost more than double the supply voltage but at this peak we can maintain the unity power factor and this is the main motive of the proposed converter circuit to maintain or correct the power factor at high voltage to give the quality power supply.

And we will compare it with the ideal power supply with the conversion of its AC supply to DC supply by ideal diodes this shows that the output of the proposed circuit is feasible.

Now we will discuss this comparison with detailed circuit diagram of simulation and its output waveform of both the proposed circuit and the ideal supply circuit. at the same output voltage.

5.7.1 Proposed Circuit With RL Load.

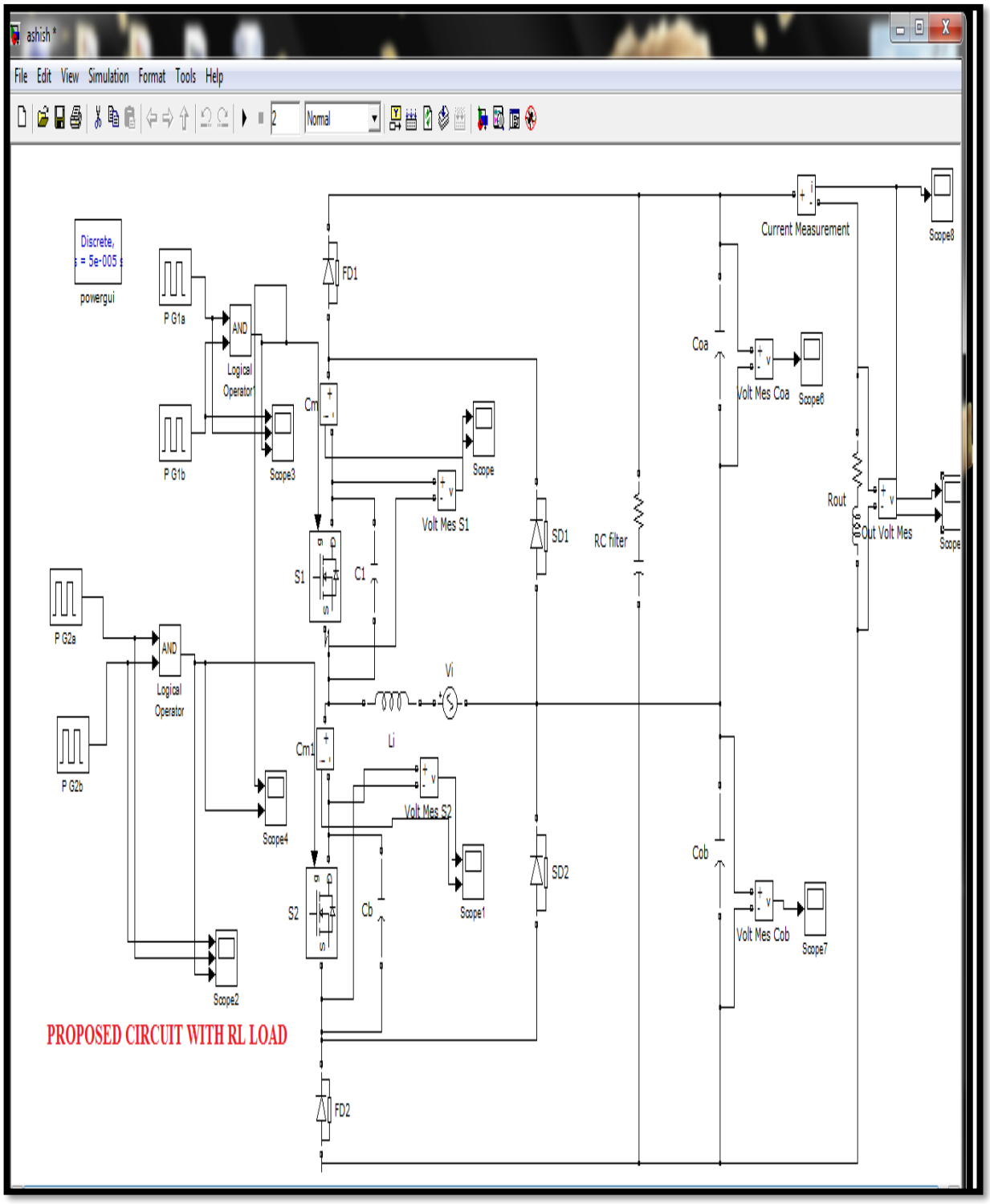

Fig.5.10. proposed circuit with RL load.

The above figure is given of the simulation which is designed in SIMULINK and its output signal given to the scope can be obtained and analysed from the scope. Different

scope is for different output signal waveform its detailed description is given in the next page.

5.7.2 Output Waveform with RL Load.

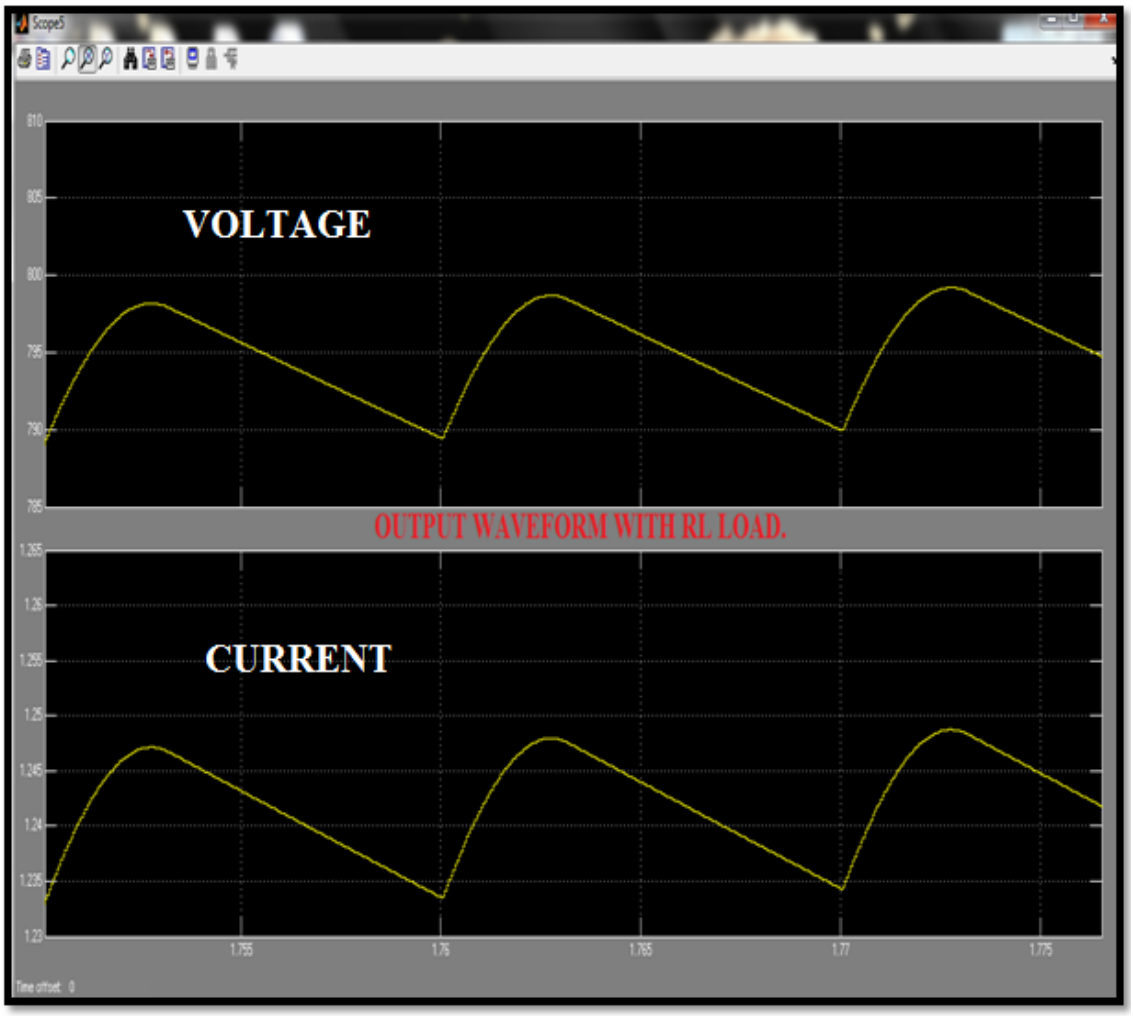

Fig. 5.11 output waveform of RL load

The above figure shows the output waveform of the proposed circuit with RL load this output wave form shows that the power factor of the load is of unity power factor which is dam clear from the above figure in which the output wave form is given.

Now we will discuss about the ideal circuit which takes the ideal supply and uses the ideal diode so its output gives the ideal output waveform and this output is harmonics distortion frees, smooth unity power factor output which is same as of the output of the proposed converter circuit. Next is the circuit and load waveform of the ideal circuit.

5.7.2 Ideal Supply Circuit.

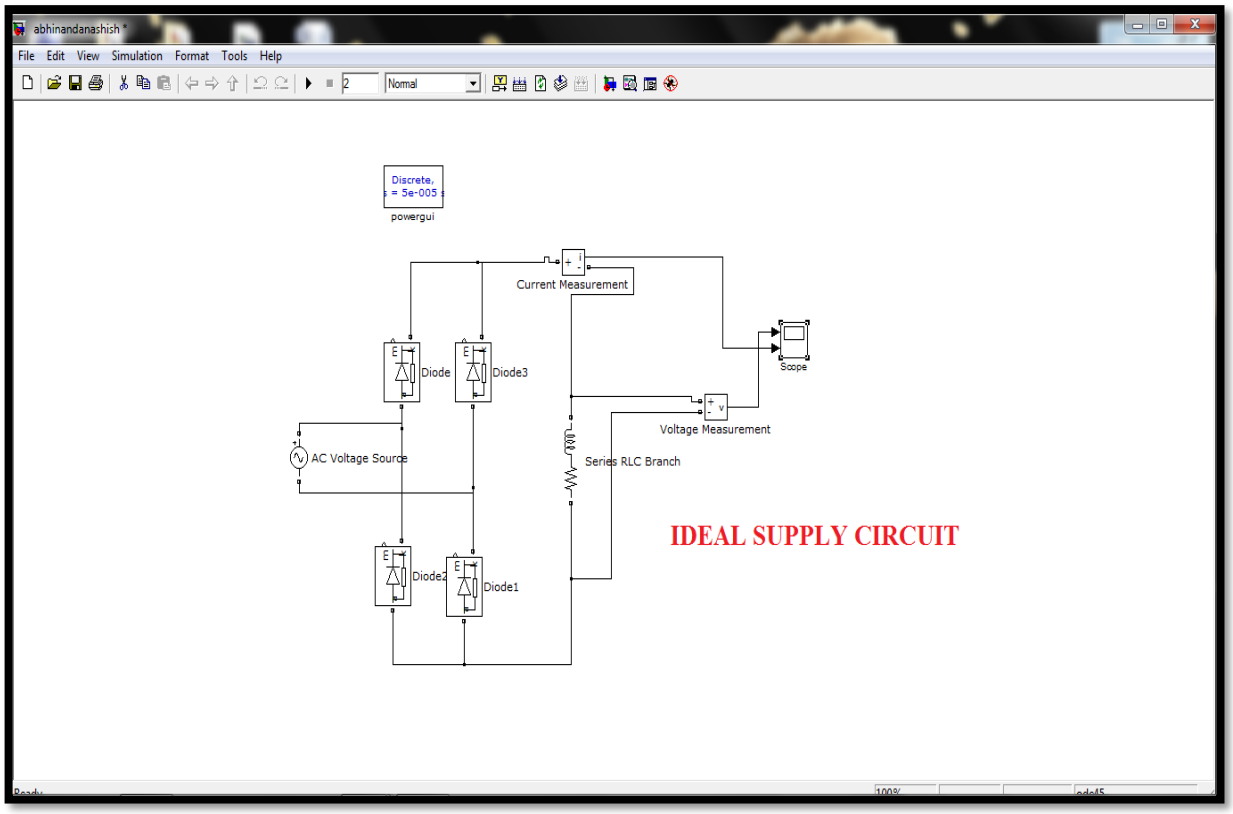

Fig.5.12. Ideal supply circuit.

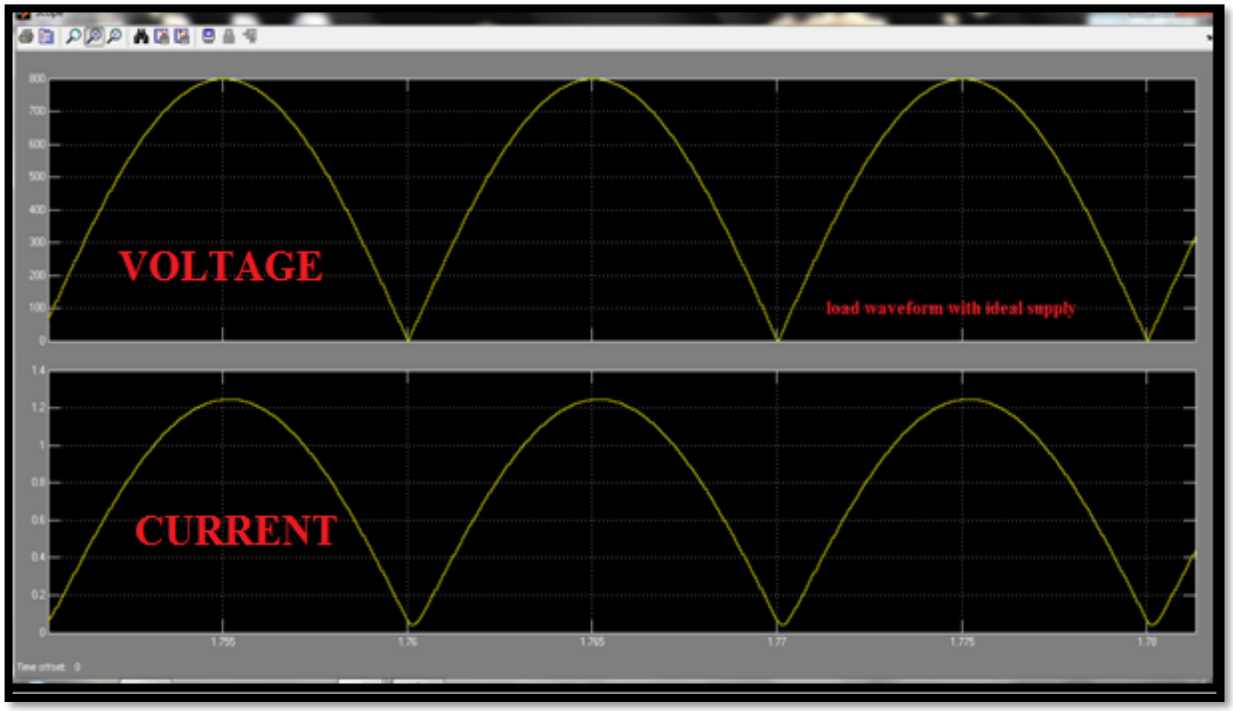

Fig.5.13 Ideal output waveform

The above figure output is of ideal source which is of unity power factor and the harmonics, ripple free output and the proposed circuit output is also of unity power factor and ripple free output.

This shows that the proposed converter circuit gives the unity power factor with the slow diode which acts as rectifier and nature voltage clamp and this is the similar condition to the ideal circuit supply which has also discussed.

This is the overall condition for the comparison of the proposed circuit with the ideal supply circuit. So from this it is clear that the output of the proposed circuit is feasible.

CHAPTER 6

APPLICATION OF PROPOSED CONVERTER

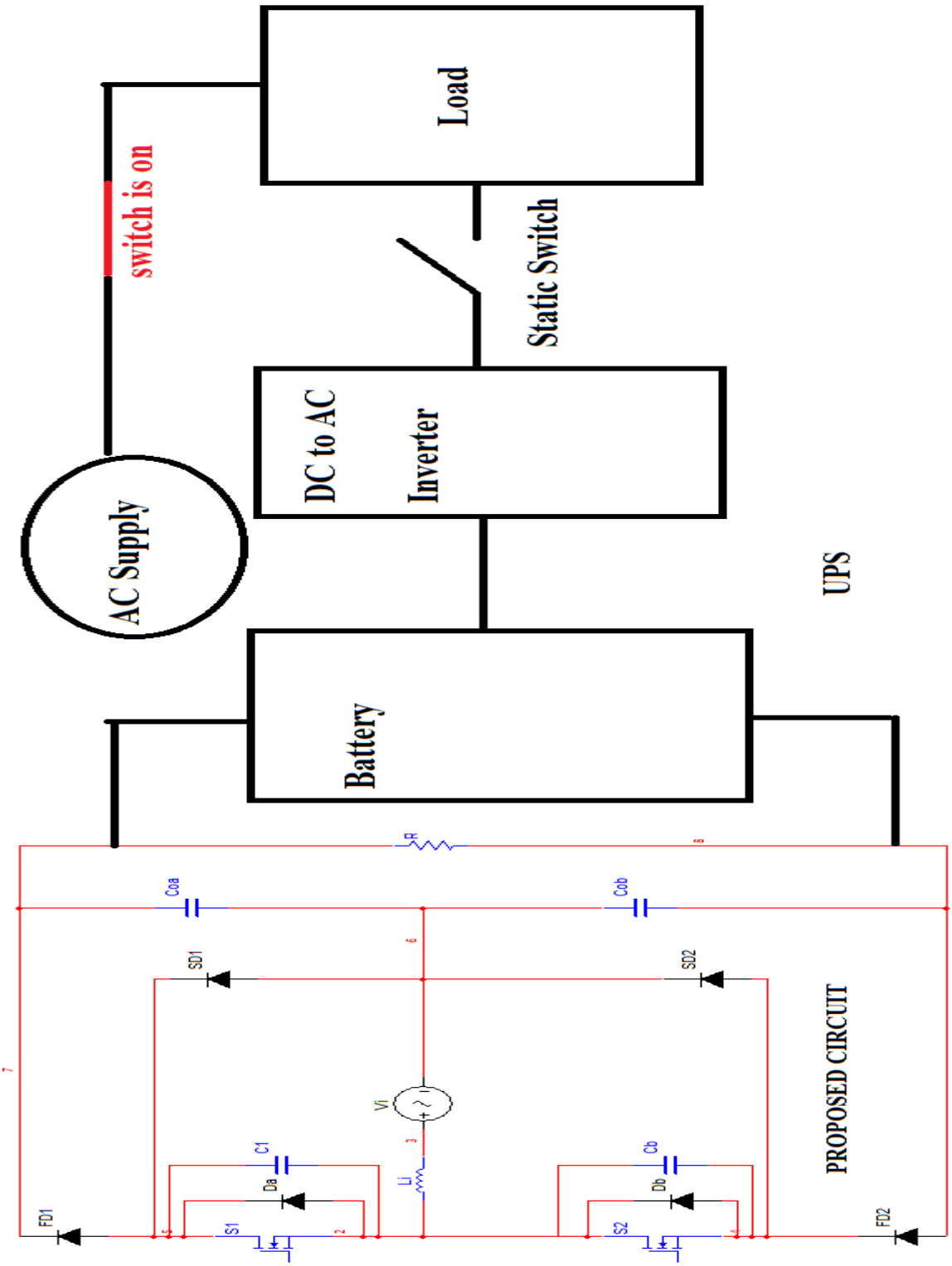

Fig.6.1. Implementation of UPS with proposed circuit

The above figure shows the implementation of the uninterruptable power supply (UPS) with the proposed circuit. In which UPS is fed from the three level bridgeless boost power factor corrections with nature voltage clamp.

By this when it takes input from that proposed converter circuit it takes smooth, harmonics distortion free power supply of 800V and 1.25A current and by this the battery of the UPS goes to the ideal charging because this is the good condition of charging and gives the AC output of 230V and since it fed from the ideal power of unity power factor, so the losses and the stresses on the power electronics devices will also be least. Conduction loss reduces and the heating problem by electrical loss will also be checked by ZVS and ZCS because it reduces the conduction mode losses.

And hence the efficiency of the battery of the UPS system goes on increasing and by this the device which is connected from the output of the Uninterruptable Power Supply (UPS) system performs at their best and gives its optimum efficiency.

Where it can be used?

It can be used in the offices, labs, or in the hospitals where the uninterrupted quality power supply is needed. To operate the life support system installed in the ICUs of the hospitals.

It can also be used in the railway reservation system where uninterrupted power supply is needed especially in case of TATKAL reservation period.

These are the practical daily life benefits from these proposed converter circuit.

CHAPTER 7

CONCLUSION & FUTURE WORK

7.1 Conclusion.

A single inductor three-level boost bridgeless power factor correction rectifier with nature voltage clamp characteristics has proposed in this thesis work.

In the proposed converter circuit two slow diodes are used as clamping diode and rectifier diode simultaneously. Though the slow diode and the intrinsic diode of the MOSFET operates with the switching frequency. So the problem of the reverse recovery has short out. The voltage stress of all the power electronic devices is reduced to ½ of the total output. With achievement of nature voltage clamping.

Its use with the UPS shows its versatility in field of the power system.

Circuit has some advantages.

(a). It requires only one inductor.

(b). Low voltage stress with nature voltage clamp.

(c). Low conduction losses and low CM noise.

(d). Utilization factor of device is high.

7.2 Future work.

It is well known that the demand of electricity will never be decrease in fact it will increase day by day in the coming future so this proposed circuit of the power factor correction will give birth to many demand in the arena of power system to supply a quality power which will without any harmonic distortions, voltage fluctuation. it can be used in the following manner.

This circuit can be implementing into the hardware for becoming the versatile device to supply the quality power to the electrical machine by which the high efficiency can be achieved.

Used in long lasting UPS and in Battery charging.

Since the power output of the proposed circuit is smooth and of the unity power factor so it will give good power supply to the UPS for quality power output and by this power the device which is to be fed by this will give its optimum performance with minimum loss. And it will also be the ideal battery charger for larger battery backup. Which will come in demand in the coming future?

And this is the vision for future related to this proposed circuit which will support the power system to reduce the losses and increase the efficiency.

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