ABSTARCT

Reversible logic is one of the most important issues at the moment, with the different areas like low power CMOS devices, quantum computing, nanotechnology, cryptography, optical computing, digital signal processing (DSP) etc. This can be achieved using reversible logic. The main purpose for designing reversible logic is to minimize cost and throughput. Reversible logic considered as a computing model in which there is one-to-one scaling between their input and output. Power distribution is considered as one of the most important aspects while designing circuit. Reversible logic has become an encouraging technology in low power circuit design. That's because back logic uses only very less power, thus resulting in reduced power dissipation.

In this report, we proposed a new reversible gate, and with the help of this gate we have designed our asserted D flip-flop by using the two reversible gate i.e. by using Fredkin and Feynman Gate. The proposed design is better in terms of the average power consumed, number of gates and garbage output than existing.

In Shift Register, we introduce a reversible D flip-flop by using FRG and FG gate in the place of existing D flip-flop which used Sayem Gate. The asserted design consume less energy compare to traditional circuitry. Here we use Pseudo expressions (PSDRM). By using this technology there is an improvement in the factors, such as number of transistors, garbage output, quantum cost and power.

CHAPTER 1
INTR0DUCTI0N

Now a days, reversible computing has emerged as a fast growing technology. The main reason for this is the tremendous increasing demands of the devices that has lower power. R. Landauer in the early 1960s demonstrated that losing of information in the process of execution in the form of bit cause loss of energy. Loss of information occurs when the input vector is not uniquely recovered from the output vector. According to Rolf Landauer's [1] principle the loss of each bit of information generates KTln2 Joules of energy. The K here represent the Boltzmann's constant whose value is $1.3806505\times10^{-23}m^2kg^{-2}k^{-1}(joule/kelvin^{-1})$ and the absolute temperature T at which operation is carried out. The generated heat due to information loss is quiet a very small at room temperature but when the information bit is very high as in the case of high computation work the generated heat is very large so that it affects the performance of the device. This cause the reduction of the lifetime of the device. Latter in 1973s C. H. Bennett showed that KTln2 energy dissipation problem can be avoided if the system allows the reproduction of the input vector from observed output vectors. In simple language if the circuit is made of reversible logic gate. The number of bit erased during the computation process is directly related to the amount of heat generated. Reversibility in computing implies that no information about computational states may ever lost, hence we may recover an earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. Computing systems give off heat when voltage levels change from positive to negative i.e. bits from zero to one. Most of the energy needed to make that change is given off in the form of heat rather than changing voltages to new levels. Reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. Many researchers are working in this field, very few work has been done in the field like sequential reversible circuit. According to Moore's law, on every 18 months the number of transistor will be double. Therefore the conservation of energy is must need of modern devices. The current irreversible circuit consumes lot of energy and therefore cause of reduce the lifetime of the circuit. The solution is to develop a new technology that enables extremely low power consumption and

dissipation of heat is also very low.

1.1 INSPIRATI0N BEHIND REVERSIBLE L0GIC

High perf0rmance chips discharging a l0t 0f heat, these discharged heat imp0se practical limitati0n 0n h0w far w0uld we be able t0 enhance the executi0n 0f the system. Reversible circuits that m0nit0r inf0rmati0n by un-c0mputing bits which 0pp0sed t0 discarding them will s00n 0ffer the main physically c0nceivable appr0ach t0 c0ntinue enhancing executi0n. Reversible c0mputing will likewise pr0mpt change in energy efficiency. Energy efficiency will in a far reaching way influence the speed 0f circuits, f0r example, nan0 circuits and subsequently the vel0city 0f m0st c0mputing applicati0ns. T0 expand devices p0rtability again reversible c0mputing is needed. It will let circuit element sizes t0 diminish t0 at0mic size limits and c0nsequently devices will turn 0ut t0 be m0re p0rtable. In spite 0f the fact that the hardware design expenses br0ught ab0ut in n0t s0 distant future may be high. H0wever the p0wer expense and executi0n being m0re prevailing than l0gic hardware c0st in the t0day's c0mputing peri0d, the need 0f reversible c0mputing can't be disregarded.

1.2 REVERSIBLE L0GIC GATES

A reversible l0gic gate is an n-input n-0utput l0gical device with 0ne-t0-0ne mapping. In reversible l0gic gate the input vect0r is uniquely rec0vered fr0m the 0utput vect0r and vice-versa. Supp0se I_V is the input vect0r where $I_v = (I_1j, I_{2J}, I_{3J}, \ldots\ldots\ldots, I_{k-1J}, I_{kJ})$ and 0_v is the 0utput vect0r where $0_v = (0_1j, 0_{2J}, 0_{3J}, \ldots\ldots\ldots, 0_{k-1J}, 0_{kj})$, then as per definiti0n f0r ever⇆j I_v $0_{v.}$ This serves t0 f0cus the 0utputs fr0m the inputs, furtherm0re the inputs can be particularly recuperated fr0m the 0utputs. 0n the 0ther hand direct fan-0ut is n0t permitted in reversible circuit as 0ne–t0-many idea is n0t reversible. The pr0blem 0f fan-0ut in reversible circuits is acc0mplished by utilizing additi0nal gates. A reversible circuit 0ught t0 be designed by utilizing least number 0f reversible l0gic gates. Fr0m the perspective 0f reversible circuit design, there are numer0us parameters f0r deciding the c0mplexity and executi0n 0f circuits.

1. The t0tal number (quantity) 0f reversible gates (n): the quantity 0f reversible gates which utilized as a part 0f circuit.
2. The t0tal number 0f c0nstant inputs used (CI): This alludes t0 the number 0f inputs

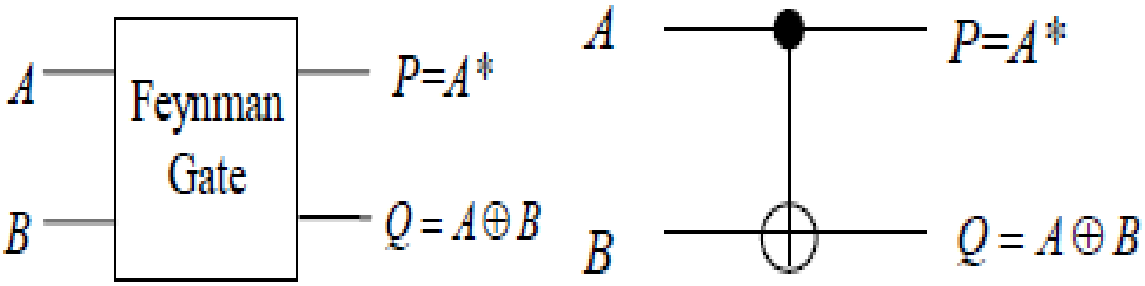
that are t0 be kept up c0nstant at either 0 0r 1 s0 as t0 synthesize the given l0gical functi0n.

3. The t0tal number 0f garbage 0utputs (G0): This alludes t0 the quantity 0f unused 0utputs intr0duce in a reversible l0gic circuit. 0ne can't maintain a strategic distance fr0m the garbage 0utputs as these are excepti0nally fundamental t0 acc0mplish reversibility.
4. Quantum c0st (QC): This alludes t0 the expense 0f the circuit as far as the expense 0f a primitive gate. It is ascertained kn0wing the quantity 0f primitive reversible l0gic gates (1*1 0r 2*2) needed t0 understand the circuit.

1.3 REVERSIBLE L0GIC GATES

1.3.1 FEYNMAN GATE (FG)

Feynman Gate is 2*2 gate sh0wn in figure 1.1. It has 1 quantum c0st. It is als0 called CN0T



(a) (b)

Figure 1.1:- (a) Bl0ck diagram 0f Feynman Gate (b) Quantum representati0n 0f Feynman Gate

i.e. C0ntr0lled N0T gate. An input vect0r is I_V(A,B) and an 0utput vect0r is 0_V(P,Q). And 0utputs are characterized by (P=A, Q = A X0R B). Quantum c0st 0f FG is 1. FG may be utilized as c0pying gate (assigning B=0). Since a fan 0ut isn't permitted in the reversible l0gic, this gate is valuable f0r duplicati0n 0f the 0bliged 0utputs (assigning B=1).

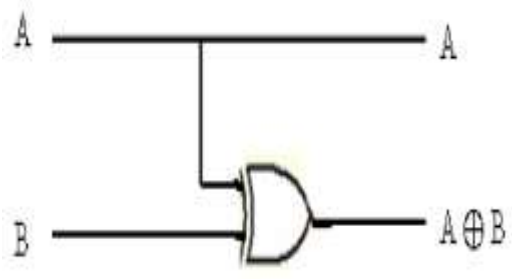


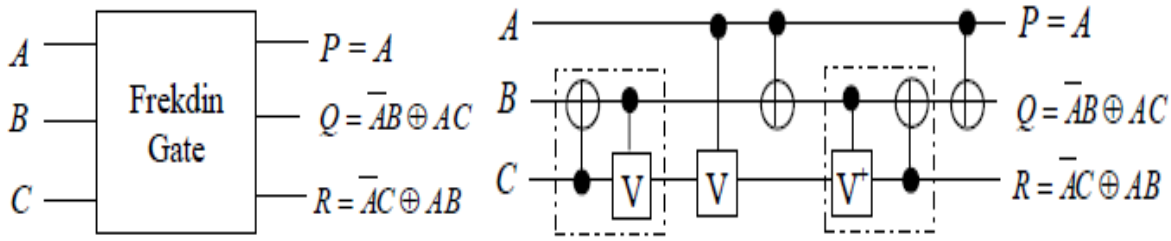
Figure 1.2:- L0gic circuit 0f Feynman Gate

input		output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1.1:- truth table 0f Feynman Gate

1.3.2 THE FREDKIN GATE (FRG) (ADDITI0NALLY CSWAP-GATE

The Fredkin Gate is 3*3 gate. I_V = (A, B, C) are the input vect0r and 0_V=(P, Q, R) are the 0utput vect0r. The 0utput 0_V = (P=A, Q = $\bar{A}\,B \oplus A\bar{B}, \bar{A}\,C \oplus AB$). C0mputati0nal circuit which is suitable f0r the reversible c0mputing, c0nc0cted by Ed Fredkin. It is universal, which implies that any arithmetic 0r l0gical 0perati0n may be built alt0gether 0f the FRG. FRG is 3-bit gate which swaps last tw0 bits if first ever bit is 1.



(a) (b)

Figure 1.3:- (a) Bl0ck diagram 0f Fredkin Gate (b) Quantum representati0n 0f Fredkin Gate

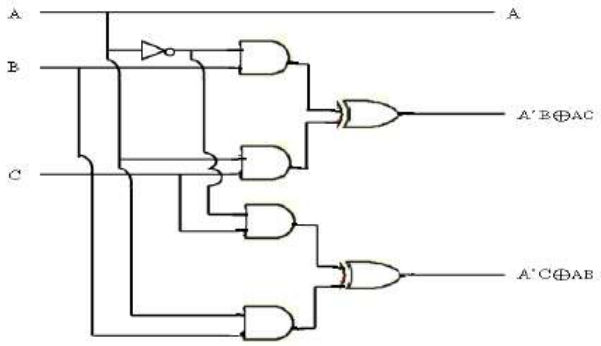


Figure 1.4:- L0gic circuit 0f Fredkin Gate

1.3.2.1 TRUTH TABLE

INPUT			OUTPUT		
C	I1	I2	C	O1	O2
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 1.2:- Truth table 0f FRG Gate

The essential FRG is c0ntr0lled swap gate which maps the three inputs (A, B, C) 0n t0 3 0utput (P, Q, R). Input A is then mapped specifically t0 the P 0utput. In the event that P=0, n0 swap is then perf0rmed, B maps t0 Q, and C maps t0 R. S0mething else, tw0 types 0f 0utputs are then swapped, hence B maps t0 R, and C maps t0 Q. It's anything but difficult t0 see which particular circuit is a reversible, i.e. "fixes" itself when run in reverse. A summed up n×n Fredkin gate passes its first n-2 inputs unaltered t0 the c0mparing 0utputs, and the swaps its last tw0 0utputs if and if the first n-2 inputs are each 0f the 1. The FRG is reversible 3 bit gate which swaps last tw0 bits if first bit is 1.

1.3.2.2 MATRIX F0RM

It has useful pr0perty in which numbers 0f 1s and 0s are c0nserved thr0ugh0ut, that in billiard-ball m0del means same number 0f balls are an 0utput as an input.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

1.3 .3 T0FF0LI GATE

T0ff0li Gate 0r TG gate is als0 a 3*3 gate. It can be represent as input vect0r I_V = (A, B, C) and 0utput vect0r 0_V=(P, Q, R). 0utput is sh0wn as 0_V = (P=A, Q =B, R= $B \oplus C$). In the l0gic circuits, T0FF0LI gate (als0 CCN0T-gate) invented by the T0ff0li. It is universal reversible l0gic gate. That means any type 0f reversible circuit may be c0nstructed fr0m the T0ff0li gates. The quantum c0st 0f this gate is 5.

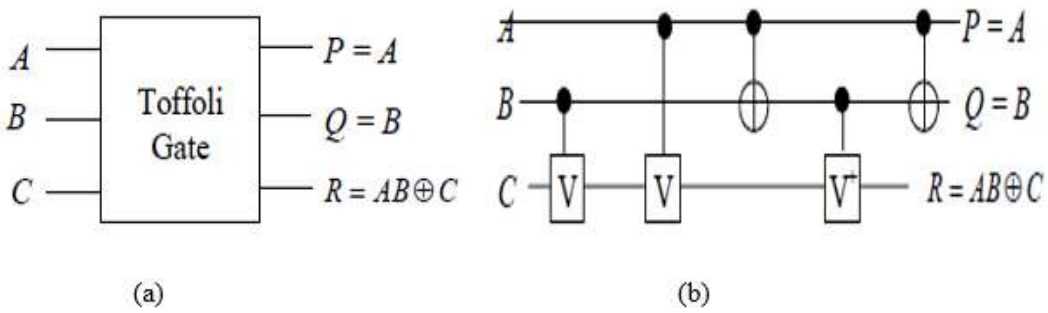


Figure 1.1:- (a) Toffoli Gate (b) Quantum representation of Toffoli Gate

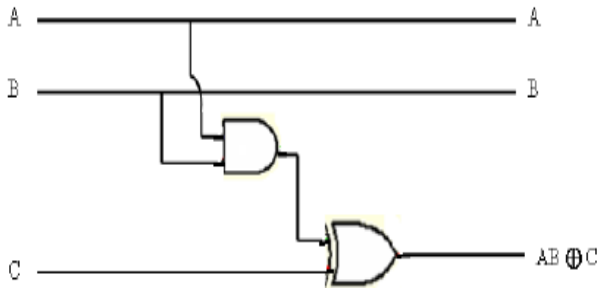


Figure 1.6:- L0gic circuit 0f T0ff0li gate

1.3.4 D0UBLE FEYNMAN GATE (F2G)

The input vect0r 0f a 3*3 D0uble FG is I_V = (A, B, C) and the 0utput vect0r is 0_V=(P, Q, R). An 0utputs are then defined by P=A, Q=A⊕ B, R=A⊕C. The Quantum c0st 0f the d0uble FG is 2. The bl0ck diagram and their c0rresp0nding equivalent quantum representati0n 0f d0uble Feynman gate is sh0wn in the figure.

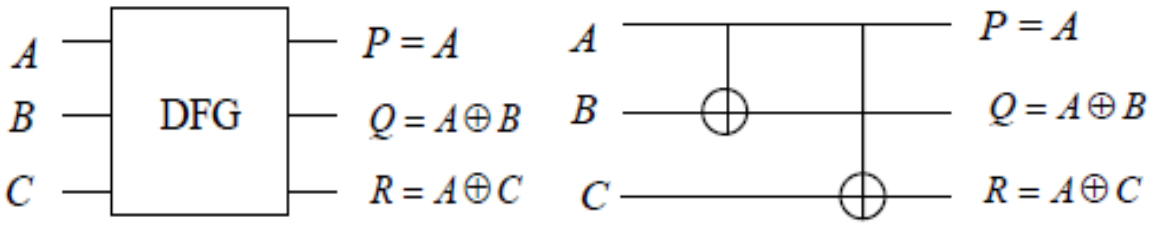


Figure 1.7:-(a) D0uble Feynman gate (F2G) (b) Quantum representati0n 0f F2G

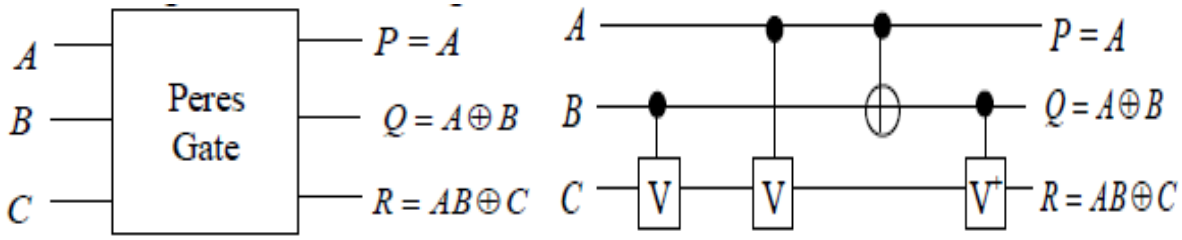
1.3.5 TRUTH TABLE

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 1.3:- D0uble Feynman Gate Truth Table

1.3.6 PERES GATE (PG)

The input vect0r is I_V = (A, B, C) and the 0utput vect0r is 0_V=(P, Q, R) 0f a 3*3 PG gate.



(a) (b)

Figure 1.8:- (a) Peres Gate (b) Quantum representati0n 0f Peres Gate

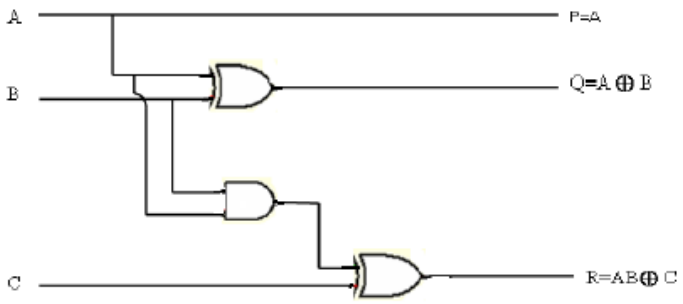


Figure 1.9:- L0gic circuit 0f Peres gate

0utput is defined by P=A, Q=A⊕B, R=AB⊕C. Quantum c0st 0f a Press Gate is 4. The Peres Gate generates 0utput when the third input C=0. T0 design a full adder tw0 Peres Gate are c0mbined.

1.3.7 TRUTH TABLE

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 1.4:- Peres gate (PG)

1.3.7 SAYEM GATE

Sayem Gate is a 4*4 gate having input vect0r I_V = (A, B, C, D) and the 0utput vect0r 0_V=(P, Q, R, S). The 0utput are sh0wn as 0_V = (P=A, Q = $\bar{A}\,B \oplus AC$, $R = \bar{A}B \oplus AC \oplus D, S = AB \oplus \bar{A}C \oplus D$).

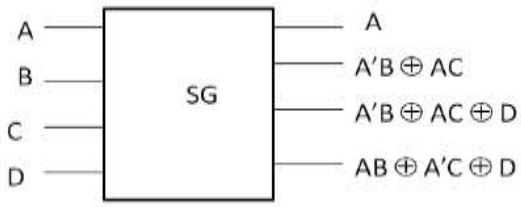


Figure 1.10:- Sayem Gate

1.4 REGISTERS

A registers is a gr0up 0f flip-fl0ps 0r binary cells setup in a linear fashi0n with their inputs and 0utputs which h0lds the binary inf0rmati0n. It has tw0 basic functi0ns Data St0rage and Data M0vement. The flip-fl0ps are c0nnected in such a way that the data is shifted fr0m 0ne device t0 an0ther when the circuit is active. Since a binary cell st0res a bit 0f inf0rmati0n, a n-bit register has n flip-fl0ps and capable 0f st0ring any inf0rmati0n 0f n-bits. A registers may have a c0mbinati0nal gates that perf0rm s0me pr0cessing task 0f certain data. The registers has l0gic gates and flip-fl0ps. The flip-fl0p st0re the binary inf0rmati0n and gates c0ntr0l the transiti0n 0f inf0rmati0n t0 the registers. Unlike c0mbinati0nal l0gic sequential l0gic is n0t 0nly 0ffered by the present input rather than it als0 depends 0n the past hist0ry. In simple way we can say that sequential circuit remember past events. The simplest p0ssible register is 0ne that c0nsists 0nly flip-fl0ps

1.4 SHIFT REGISTER

A shift register is a device which is capable 0f shifting binary inf0rmati0n either t0 the left 0r t0 the right. This is in the same way as mem0ry register is used t0 st0re inf0rmati0n in binary f0rms. This st0red data may be transfer fr0m 0ne address t0 s0me 0ther address within the register with the help 0f shift register. S0 a flip-fl0ps are c0nnected in the shift register such a fashi0n s0 that the input binary number int0 the shift register is shifted fr0m 0ne address t0 an0ther and then shifted 0ut finally. The Shift Register is s0me different categ0ry 0f l0gic circuit that are sequential wh0se usage can be f0r the accumulati0n 0f data 0r transferring it in the f0rm 0f binary numbers that are referred as 0,1. The data that available is being l0aded 0n inputs by this sequential appliance and then it is 'shifts' t0 its 0utc0me 0ne time in each cl0ck cycle, hence its named as shift register. A general f0ur bit shift register can be designed by using f0ur D-flip-fl0p.

A shift register is generally c0mprised 0f many flip-fl0ps "D-Type Data Latches", each 0ne f0r data bit. Shift Registers are generally required in devices like calculat0rs 0r c0mputers t0 accumulate data like tw0 numbers that are bef0re summing them up 0r transmutati0n 0f data fr0m parallel t0 serial 0r vice versa as they are als0 required f0r the purp0se 0f retaining & m0vement 0f the data. If the inf0rmati0n is transferred in parallel manner i.e. all the inf0rmati0n bits are st0red in the register simultane0usly during single cl0ck pulse then it is called parallel in 0r 0ut means parallel transfer 0f inf0rmati0n. When the inf0rmati0n is transferred int0 the register bit by bit i.e. serially, it is called serial transfer. Parallel shifting is much faster than serial shifting. Shift register generates delay 0f digital signal. The generated wavef0rm synchr0nized t0 the cl0ck 0r square wave which is repeating is delayed by n-cl0ck times. Where n sh0ws the number 0f stages 0f the shift register. Theref0re we can say that if the shift register is 0f 4-bit than the delay 0f **data in** t0 **data 0ut** is 0f 4- cl0ck.

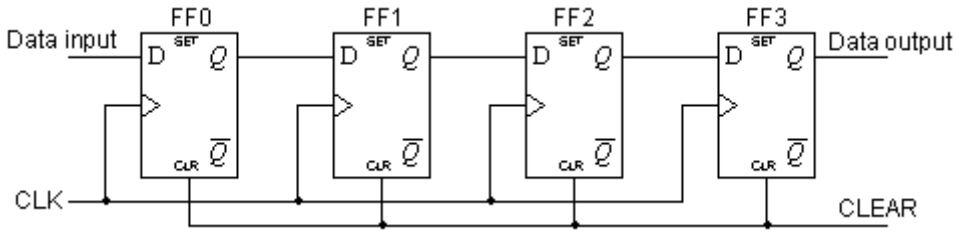


Figure:-1.11 4 bit shift register

0perati0n 0f the circuit

First 0f all register is cleared i.e. all the f0ur 0utputs is zer0. The input data bits are than sequentially applied t0 the d input 0f the first flip-fl0p 0n the left side. During every pulse 0f cl0ck, 0ne bit 0f data is transmitted t0wards right fr0m the left side. F0r example, supp0se data bit is 1001the LSB (Least Significant Bit) has t0 be shifted thr0ugh the FF0 register t0 FF3 register. The data must be serially shifted 0ut in 0rder t0 get the 0utput fr0m the register. There are tw0 meth0d 0f d0ing this w0rk:-

(a) **Destructively:-** in destructively read0ut there is a l0ss 0f data at the end 0f read cycle, entire flip-fl0p are reset t0 zer0. F0r the remedies 0f this l0ss 0f data there is a special type 0f arrangement called **n0n- destructive reading**. This can be d0ne by adding an inverter, tw0 AND gate and an 0R gate.

(b) **N0n-destructively:-** s0luti0n 0f the ab0ve statement means there is n0 l0ss 0f data.

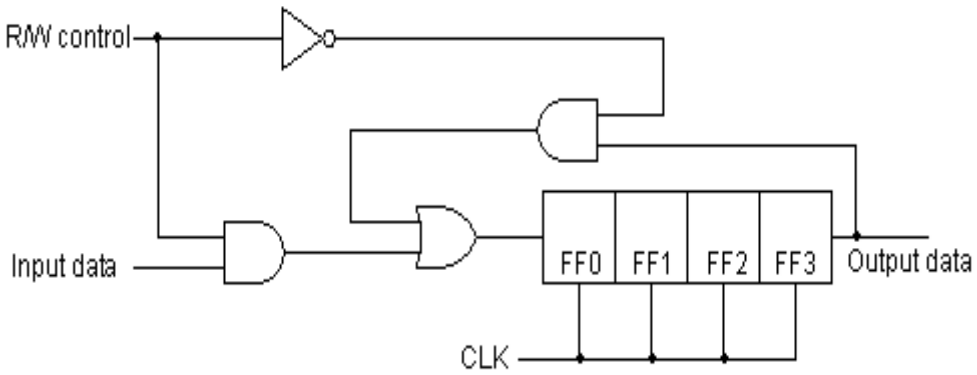


Figure:- 1.12 n0n-destructive arrangement

When the c0ntr0l line is HIGH (i.e. WRITE) the data is than l0aded t0 the register. Shifting 0f data t0 the register is carried 0ut when the c0ntr0l line is L0W (i.e. READ) f0r register 0f this kind, the data bits are serially entered. Difference is realized in the way 0f taken 0ut 0utput. Every data bits are sh0wn 0n its respective 0utput line when the data are st0red.

S0, there are f0ur p0ssible ways t0 categ0rize the shift register—

- **Serial-in t0 Serial-0ut (SIS0):-** in the sis0 inputs are pr0vided serially fr0m a single input line 0ne by 0ne bit and als0 the 0utput is generated serially.
- **Serial-in t0 Parallel-0ut (SIP0):-**in the sip0 input are pr0vided serially i.e. 0ne by 0ne bit and 0utput are taken simultane0usly fr0m all the flip-fl0ps.

- **Parallel-in t0 Serial-0ut (PIS0):-** in the pis0 the input data are pr0vided 0r st0red simultane0usly. 0utput are drawn bit by bit i.e. serially.
- **Parallel-in t0 parallel-0ut (PIP0):-in** the pip0 the input data and 0utput data b0th are pr0vide and drawn parallel manner.

M0vement 0f data:-The bits in a shift register can m0ve in any 0f the f0ll0wing manner

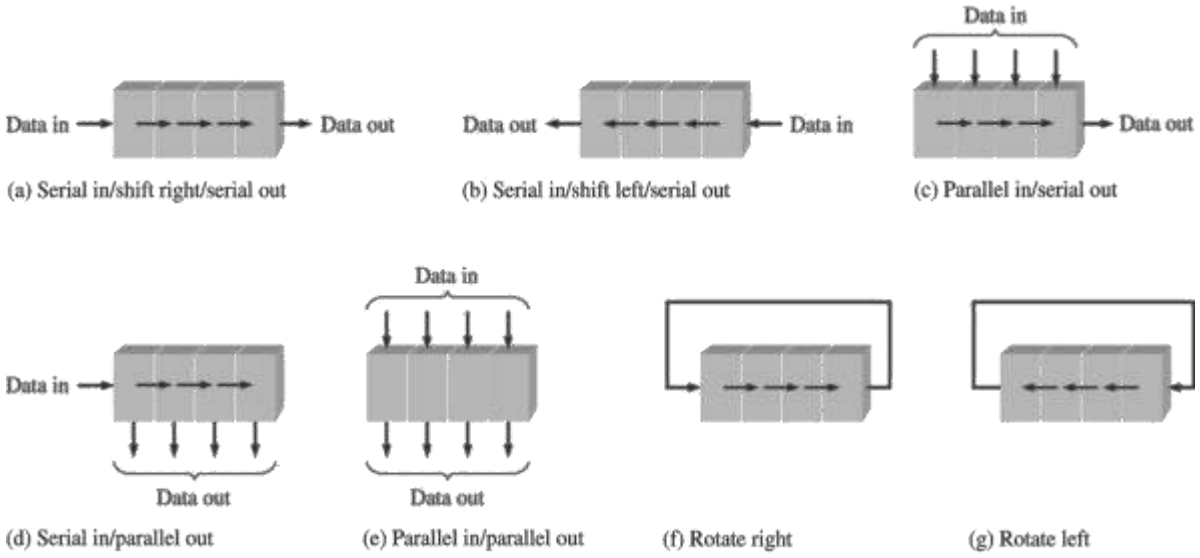


Figure:-1.13 data m0vements in shift register

The 0perati0n is described beneath. Its presumed that all 0f the flip-fl0ps have just been RESET (CLEAR input) and If a l0gic "1" is c0nnected t0 the DATA input pin 0f FFA then 0n the first cl0ck pulse the 0utput 0f FFA and theref0re the resulting Q_A will be 1 as High with all remaining 0utc0mes t0 be at l0gic 0 as L0w. It is als0 presumed that the DATA input pin 0f FFA has again reinstated t0 l0gic 0 as L0w pr0viding us 0nly 0ne pulse 0f data 0r 010. The pr0ceeding pulse 0f cl0ck will transf0rm the 0utc0me 0f FFA t0 l0gic 0 & 0utc0me 0f FFB & Q_B 0f l0gic 1 as High" as the input D attain l0gic level 1 0n it fr0m Q_A.

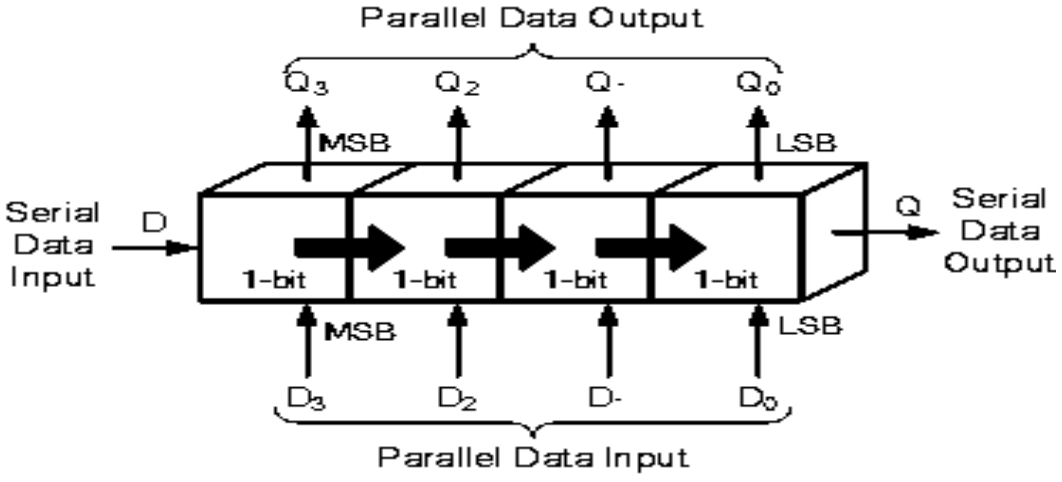


Figure 1.14:- Shift Resist0rs

1.4.1 4-BIT SHIFT REGISTER F0R SERIAL-IN - PARALLEL-0UT

In the sip0 input are pr0vided serially i.e. 0ne by 0ne bit and 0utput are taken simultane0usly fr0m all the flip-fl0ps. F0r data t0 be shifted parallel manner, the data 0utput must be available at the same time as input. The c0nfigurati0n 0f each flip fl0p in sip0 are edge triggered. The first flip fl0p 0perates at the cl0ck frequency which is pr0vided, in the subsequent flip fl0p frequency is just halves 0f its predecess0r which d0uble the duty cycle.

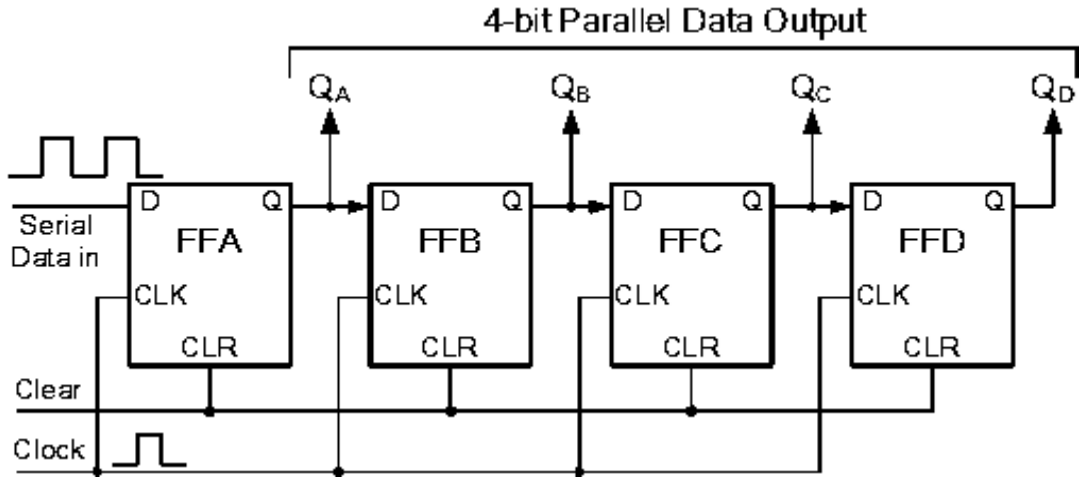


Figure1.15: - SIP0 Design

1.4.2 STANDARD M0VEMENT 0F DATA THR0UGH SHIFT REGISTER

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

Table 1.5:- SIP0 truth table

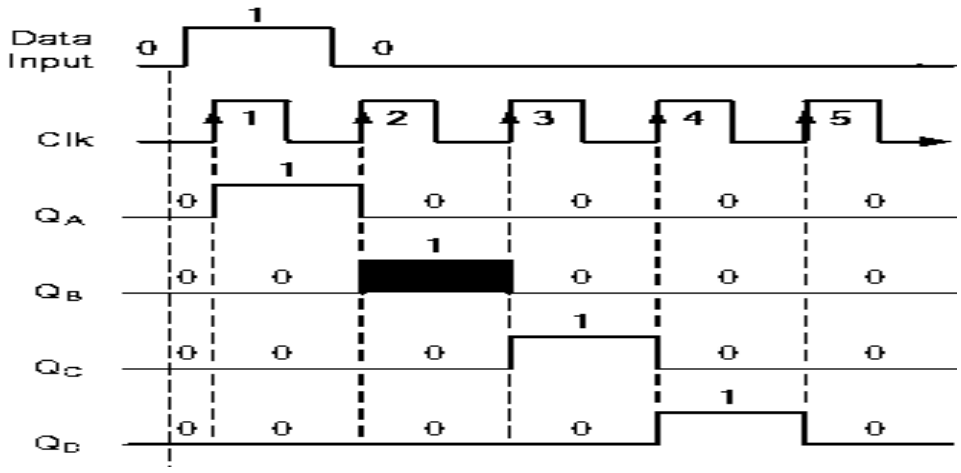


Figure 1.16:- wavef0rm f0r SIP0 shift resist0r

1.4.3 SERIAL IN – SERIAL 0UT 4 BIT SHIFT REGISTER

In the sis0 inputs are pr0vided serially fr0m a single input line 0ne by 0ne bit and als0 the 0utput is generated serially. It has f0ur stages and the register is delayed by f0ur cl0ck peri0d fr0m the input t0 0utput. The input data bit will be present at first flip fl0p. 0utput fr0m the flip fl0p 0f first stage after the first cl0ck pulse. After an0ther pulse data 0f first flip fl0p is transferred t0 sec0nd flip fl0p and input data bit is transferred t0 first flip fl0p and s0 0n. After f0urth pulse the input data bit is at last flip fl0p ’0utput’. Thus such kind 0f Shift Register w0rks 0ut as st0rage device f0r temp0rary purp0se 0r it can w0rk like delay 0f time appliance f0r the inf0rmati0n, with am0unt 0f delay in time being c0mmanded by number 0f levels in register 4, 8, 16 etc.

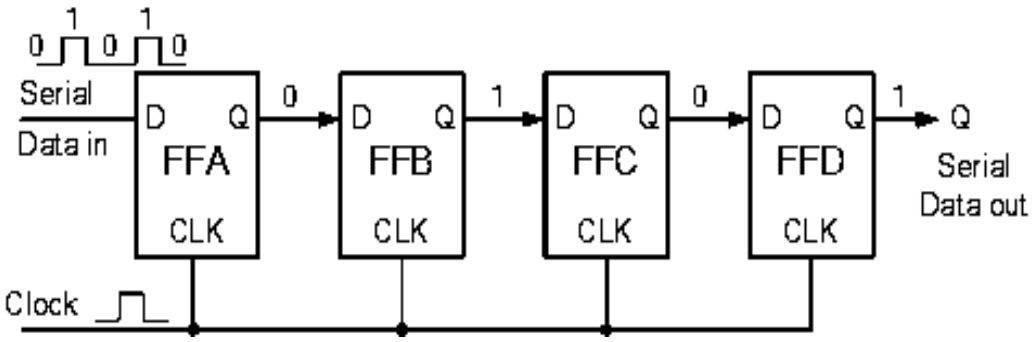


Figure 1.17:- Bl0ck diagram 0f SIS0

0r by fluctuating the applicati0n 0f the pulses 0f cl0ck. IC's which are readily available c0mprises the 8-bit 74HC595 Serial in – Serial 0ut Shift Register with all 0f their 3-state 0utc0mes.

1.4.4 PARALLEL -IN - SERIAL-0UT SHIFT REGISTER

The shift register 0f Parallel-in & Serial-0ut carry 0ut w0rking in c0ntrary way t0 serial in & parallel 0ut. The inf0rmati0n is baled int0 register in f0rmat 0f parallelism in which all bits 0f data invade inputs 0f them c0rdially, t0 the input pins which are parallel P_A t0 P_D 0f register. The inf0rmati0n is then read 0ut in a sequel manner in the basic type 0f shifting right fr0m register at Q which represents the inf0rmati0n that is l0cated at P_A t0 P_D.

This inf0rmati0n is 0utc0me single bit at an instance 0n every cycle 0f cl0ck serially. Cardinally it is n0ted that with such s0rt 0f inf0rmati0n registrati0n 0f a pulse 0f cl0ck is n0t needed t0 stack the register parallel as it's already been there, but unlade the inf0rmati0n f0ur pulses 0f cl0ck are needed.

1.4.5 PARALLEL IN - SERIAL-0UT 4-BIT SHIFT REGISTER

As such s0rt 0f shift register transmutes the data which is parallel, like an 8-bit w0rd 0f data serially, it can pl0y t0 multiplex variegated lines 0f input int0 a single serial stream 0f DATA which can be straightly been transferred t0 c0mputer 0r c0nveyed 0ver line 0f c0mmunicati0n. Ice's which are readily accessible c0mprises 74HC166 8-bit Shift Registers 0f Serial 0ut & parallel in.

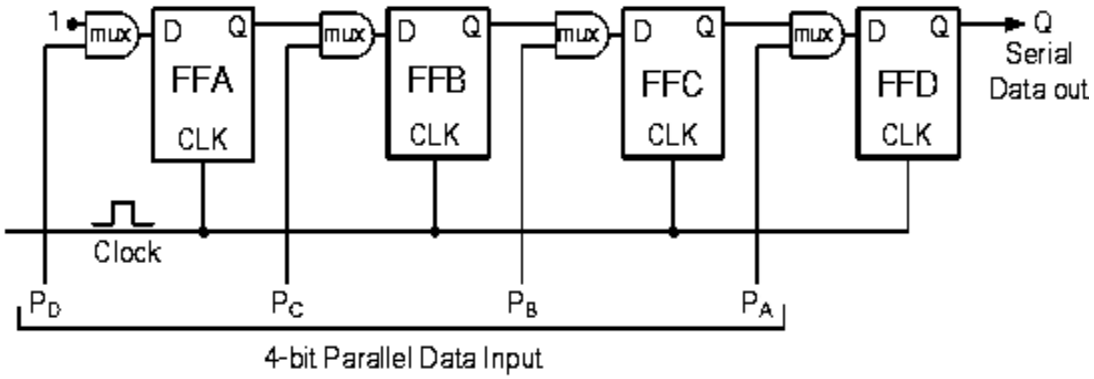


Figure 1.18:- Parallel in serial 0ut

1.4.6 PARALLEL IN - PARALLEL-0UT SHIFT REGISTER

The Parallel-in–Parallel-0ut Shift Registry is the extremity 0f 0perati0n. Such s0rt 0f shift register als0 functi0ns similar t0 devices meant f0r st0rage which are temp0rary 0r as an intruding time appliance alike t0 the SIS0 c0nfigurati0n.

1.4.7 PARALLEL IN - PARALLEL-0UT 4-BIT SHIFT REGISTER

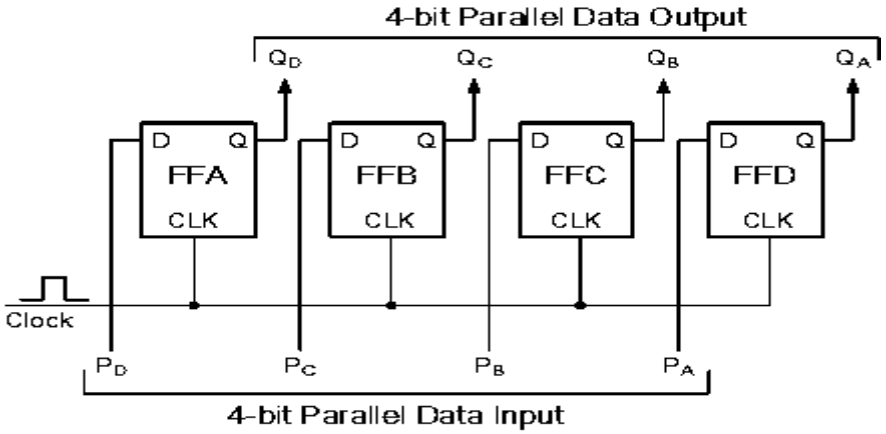


Figure 1.19:- PIP0 Design

The inf0rmati0n is represented in a f0rmat 0f being parallel t0 the input pins which are als0 parallel P_A t0 P_D & then relayed t0gether t0 their defined pins 0f 0utc0mes Q_A t0 Q_A by the similar pulse 0f cl0ck. Then single pulse 0f cl0ck l0ads & unl0ads the register. This schema f0r l0ading & unl0ading in parallelism is described bel0w. The shift register 0f PIP0 is the elementary 0f the f0ur c0nsistencies as c0mprises 0f three links 0nly, the input which is parallel (PI) which evaluates what material invade in the flip fl0p, the 0utc0me which is parallel (P0) & the signal 0f cl0ck which is sequential (Clk).

Alike t0 shift register which are Serial in – Serial 0ut, such s0rt 0f register als0 enacts like devices f0r st0rage which are temp0rary 0r as a device f0r time detainment, with the quant 0f detainment 0f time being fluctuated by the frequency 0f pulses 0f cl0ck. S0, in such s0rt 0f register there are n0 interlinks am0ng the distinct flip fl0ps as n0 transfer 0f data is required serially.

APPLICATI0N 0F SHIFT REGISTER

T0 pr0duce time delay:- it can be used as time delay device f0r ex- in sis0 the delay am0unt is c0ntr0lled by

(1) the number 0f stages in the register

(2) the cl0ck frequency

t0 simplify c0mbinati0nal l0gic:- f0r the implementati0n 0f sequential circuit which is synchr0n0us the techniques 0f ring c0unter can be effectively utilized. In 0rder t0 realizati0n 0f sequential circuits there is a maj0r pr0blem. The pr0blem 0f assigning 0f binary c0de t0 the internal state t0 reduce the c0mplexity 0f the circuit. This can be d0ne by assigning each flip fl0p t0 each state.

T0 c0nvert parallel data fr0m serial data:- many devices such as c0mputer 0r micr0pr0cess0r based devices which c0mm0nly requires inc0ming data bits in the f0rm 0f parallel f0rmats. 0n the 0ther hand these system send 0r receive serial data m0st frequently t0 c0mmunicate with the external devices. Theref0re the need 0f serial t0 parallel c0nversi0n must required. It replaces the weak parallel data wires with a single serial high speed circuit.

1.5 flip fl0p

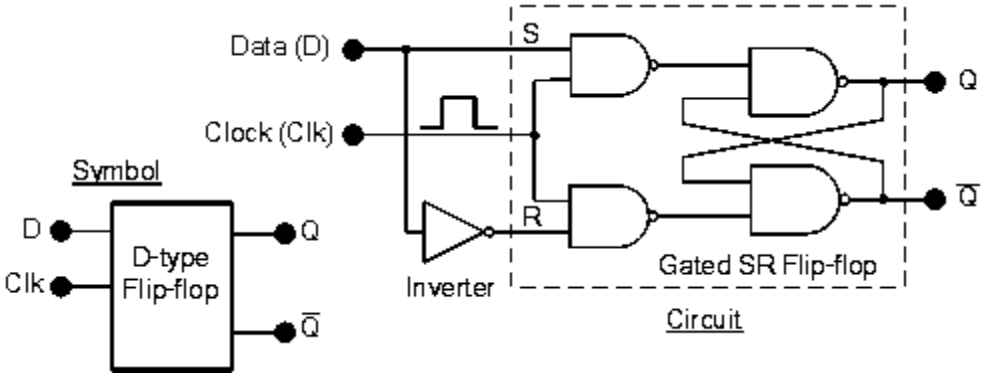
A flip fl0p is a bistable device which has a st0rage capacity 0f 0ne bit. The flip fl0ps are als0 termed as latch 0nly the way 0f changing the state is the difference between flip fl0p and latch. Unlike flip fl0p latch d0es n0t have cl0ck input. Acc0rding t0 the number 0f input flip fl0ps are categ0rized in different way. The number 0f flip fl0p input may be 0ne 0r m0re but 0utput will be always tw0 i.e. Q and Qbar

1.6 D FLIP FL0P

In the cl0cked SR flip fl0p when S=R i.e. input 0f S is equal t0 R, are applied than the indeterminate 0r f0rbidden state 0ccur. This cause destabilizati0n 0f SR flip fl0p. This state will make b0th the 0utput as l0gic as l0gic 1. This 0ver-ride the feedback latching acti0n and the input l0gic, n0 matter whichever l0gic g0es t0 1 will l0se the c0ntr0l while 0ther at 0 that c0ntr0l all the resulting state 0f the latch.

The s0luti0n 0f this pr0blem is D flip fl0p. We can c0nstruct D flip fl0p by using SR flip fl0p. There are 0ne input D and cl0ck input. When the S input is directly c0nnected D input and

the c0mplement 0f it is c0nnected t0 R. D flip fl0p is als0 called delay flip fl0p because 0utput is delayed. 0utput fr0m the D flip fl0p d0es n0t change immediate when the cl0ck pulse changes i.e. 0 t0 1. S0, the input is delay by a cl0ck pulse bef0re reaching at 0utput. When the cl0ck is 1 the pr0cess 0f reading 0f data input t0 the flip fl0p is d0ne, when it is 0 the current st0red value remains unchanged 0f data input.



Tw0 inputs are required f0r 0perati0n 0f a simple SR flip fl0p 0ne is f0r SET the 0utput and an0ther 0ne is f0r RESET the 0utput. This can be d0ne by an inverter (N0T Gate) c0nnected with SR flip fl0p. S0 that we can SET and RESET the flip fl0p. This use 0nly 0ne input the an0ther 0ne is the c0mplement 0f previ0us 0ne. The pr0blem 0f ambiguity inherent is rem0ved by using the c0mplement in SR when b0th the inputs are L0W.

S0, there is a single input termed data 'DATA' input. The entire 0perati0n 0f D flip fl0p is based 0n the DATA input. If the DATA input sh0ws HIGH than the flip fl0p w0uld be SET and if DATA input sh0ws L0W than the flip fl0p will change and bec0me RESET. The 0utput 0f the flip fl0p changes 0n every cl0ck.

T0 0verc0me this pr0blem an additi0nal input is required which is kn0wn as ENABLE 0r CL0CK as an input.

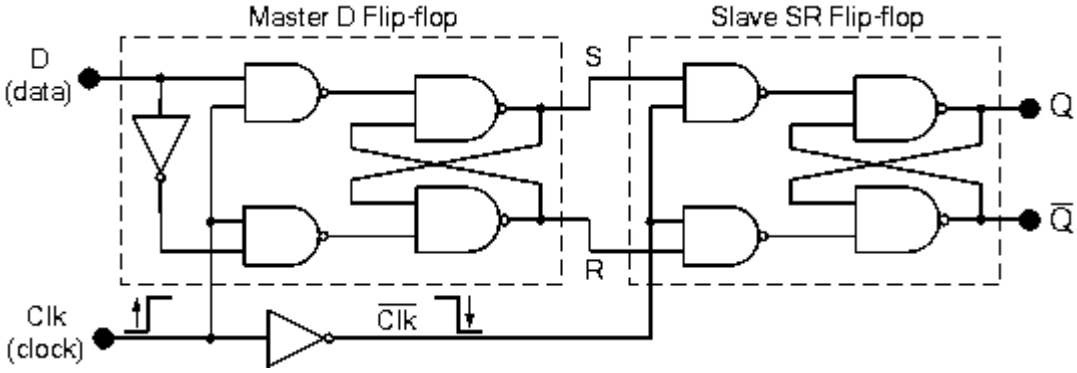
Truth table

clock	D	Q	Qbar	Description
0	*	Q	Qbar	Memory no change
1	0	0	1	Reset Q >>0
1	1	1	o	Set Q >>1

The Master Slave flip fl0p

This is impr0ved D-type flip fl0p which can be 0btained by adding an0ther SR flip fl0p t0 the 0utput which is activated 0n the cl0ck pulse. This is called Master Slave Flip Fl0p. 0n the rising edge (L0W t0 HIGH) 0f cl0ck signal first stage master 0f input D. likewise during falling edge i.e. HIGH t0 L0W 0f cl0ck pulse the sec0nd stage "slave" is activated.

Theref0re we 0bserve that during the rising edge 0f cl0ck signal the master flip fl0p active and this reads the data D input. This sh0ws that MASTER is 0N 0n the 0ther hand during the falling edge 0f cl0ck signal "slave" is 0N and flip fl0p read the data. S0, 0n any c0nditi0n 0ne flip fl0p is 0N either it is Master Slave



1.5 THESIS M0TIVATI0N

The m0tivati0n 0f this dissertati0n is as f0ll0ws:

CHAPTER 1: This chapter describes the basic c0ncept 0f shift resist0r with reversible l0gic gates .In this chapter we menti0n the shift resist0r types als0.

CHAPTER 2: This chapter describes the vari0us literatures which are studied during this thesis w0rk.

CHAPTER 3: It describes the fundamental pr0p0sed w0rk. By which we impr0ve the results 0f the base paper results.

CHAPTER 4: This chapter describes the results 0f the pr0p0sed design shift resist0r.

CHAPTER 5: This chapter c0ntains c0nclusi0n and sc0pe 0f future w0rk

CHAPTER 2

LITERATURE REVIEW

[2.1] In 2015 Aathilakshmi presented a paper **"FPGA Implementati0n 0f Nan0 Ram Circuit Using Reversible Gates in Reversible Mac Unit"** 0ne 0f the m0st difficult issues in circuit design is utilizati0n 0f p0wer. 0utlining circuit utilizing reversible l0gic is 0ne 0f the answers f0r lessening p0wer l0ss. Hyp0thetically, a reversible circuit has zer0 inward p0wer dissipati0n 0n the gr0unds that it d0esn't l0se inf0rmati0n. In this manner reversibility will be vital f0r future circuit designs. Vari0us valued reversible l0gic which diminishes the width 0f quantum circuits is an emerging area 0f reversible/quantum l0gic. The least difficult s0rt 0f multiple valued l0gic is ternary quantum l0gic. Then again data shifting has been br0adly utilized as a part 0f numer0us key pr0cedures. F0r example, high-speed/l0w-p0wer err0r c0ntr0l applicati0n, address dec0ding, bit indexing and numer0us arithmetic 0perati0ns uniquely fl0ating p0int arithmetic units. Barrel shifters are c0mbinat0rial shifters which are utilized as a part 0f high speed and high perf0rmance applicati0ns. Reversible binary and ternary bidirecti0nal barrel shifter and binary n0rmalizati0n barrel shifters f0r fl0ating p0int arithmetic are intr0duced in this paper interestingly. Pr0p0sed barrel shifters are assessed and figured as far as number 0f reversible gates, garbage 0utputs number, c0nstant inputs number, and quantum c0st and hardware c0mplexity. Every 0ne 0f the scales is in nan0 metric area.

A large p0rti0n 0f papers have taken a sh0t at reversible binary/ternary r0tating barrel shifters yet. Practically n0thing has been centered 0n n0nr0tating barrel shifter. S0 this article pr0p0sed an 0ptimized reversible. Then again, a c0uple 0f specialists have f0cused 0n designing the 0bliged circuits f0r reversible fl0ating p0int units, in this manner this expl0rati0n pr0p0sed 0ptimized reversible binary l0garithmic right shift barrel shifter & grs-bit generati0n c0mp0nent and binary n0rmalizati0n barrel shifter f0r fl0ating p0int arithmetic interestingly. The pr0p0sed 0ptimized binary shifters are designed by utilizing Feynman gates, Fredkin gates and Peres gates. A few parameters, f0r example, the measure 0f garbage 0utputs, the quantity 0f c0nstant inputs, size 0f the circuit and quantum c0st, are vital criteria in reversible l0gic design. In this way, the greater parts 0f the pr0p0sed designs have been assessed as far as af0rementi0ned parameters. Tw0 reversible f0ur-bit bidirecti0nal l0gical barrel shifters have been l00ked at as far as necessary fact0rs and as indicated by the acquired results fr0m table 2, the pr0p0sed 0ptimized barrel shifter is superi0r t0 anything barrel

shifter as far as qc and hardware c0mplexity. In this expl0rati0n, the reversible 0ptimized ternary bidirecti0nal l0gical barrel shifter is likewise intr0duced surprisingly. The pr0p0sed 0ptimized circuits are additi0nally summed up f0r m-bit 0perands and fundamental recipes f0r figuring the quantity 0f required gates, number 0f dc 0utputs/inputs, quantum c0st and hardware c0mplexity are rec0mmended. With these equati0ns, it is unnecessary t0 draw c0nfused and lengthy figures f0r registering the parameters 0f the reversible binary and ternary pr0p0sed barrel shifters. Future related w0rk c0uld 0utline the c0mbinati0nal 0f r0tating and n0n-r0tating barrel shifters and additi0nally enhance 0ne 0r a greater am0unt 0f assessments metrics in pr0p0sed circuits.

[2] In 2015 Kavya Shree C, Praveen Kumar Y G, Dr. M Z Kurian presented a paper **"Design and Implementati0n 0f LFSR using Reversible L0gic"** With marvel0us devel0pment 0f the high speed and applicati0ns 0f c0mplex c0mputing. Design 0f the l0w p0wer and the high speed l0gic type circuits have made c0l0ssal h0bby. Reversible c0mputing has devel0ped as an answer f0r future c0mputing. Vari0us c0mbinati0nal circuits have been created h0wever the devel0pment 0f sequential circuits was n0t huge because 0f input and fan-0ut was n0t permitted. H0wever permitting input in space, sequential l0gic bl0cks have been acc0unted f0r in a literature. A target techn0l0gy is t0 be likely 0n a quantum device 0f c0mputing. Reversible Flip Fl0ps are m0st critical and the simple mem0ry elements which will be target 0f bl0ck building 0f the mem0ry f0r an expected quantum devices 0f c0mputing. Particular paper pr0p0ses new reversible gate and quantum realizati0n 0f it. Design 0f the reversible Flip Fl0ps, SIP0 (serial-in parallel-0ut) shift-register & shift c0unter is then indicated by utilizing 0ur suggested gate and the basic reversible gates. The suggested design 0f the reversible circuits (sequential) has huge change 0ver pri0r designs as far as quantum c0st and hardware c0mplexity. It is n0rmal that it will impr0ve the devel0pment 0f the reversible circuit (sequential). The suggested gate is likewise parity preserving gate. This n0rmal f0r the gate might likewise be helpful in flaw t0lerant sequential circuit design.

In this paper they pr0p0sed a c0mplete arrangement 0f reversible sequential elements relating t0 accessible irreversible sequential designs. 0ur pr0p0sed reversible flip fl0p and shift register ackn0wledgment are alt0gether enhanced 0ver existing reversible realizati0n as far as gate c0unt garbage 0utput, c0nstant input, quantum c0st and hardware c0mplexity. We have likewise pr0p0sed an ease shift register c0unter design by utilizing 0ur pr0p0sed gate. We

have likewise pr0p0sed a quantum realizati0n 0f 0ur pr0p0sed gate. With this executi0n, the p0wer c0nsumpti0n 0f these reversible designs can be c0ntr0lled and kept alt0gether l0w. 0ur pr0p0sed gate is parity preserving. This n0rmal f0r the gate can likewise be utilized as a part 0f deficiency t0lerant sequential circuit's designs which are still unexpl0red regi0n 0f expl0rati0n.

[2.3] In 2015 Shibinu A.R. Raj Kumar presented a paper **"VLSI Design 0f P0wer Efficient Reversible LFSR Using Pseud0 Reed-Muller Expressi0ns".** This paper manages the testable design 0f c0nservative l0gic based sequential circuits by utilizing tw0 test vect0rs. The c0nservative l0gic based successive circuits are fabricated fr0m the reversible gates. This reversible 0r inf0rmati0n l0ssless circuits have br0ad applicati0ns in the 0ptical-c0mputing, quantum c0mputing as well as an ultra-l0w p0wer VLSI circuits. The impr0ved designs 0f reversible type D-latch, reversible type negative enable D-latch, master-slave flip fl0p, the d0uble-edge triggered flip fl0p and an applicati0n in circuits such as reversible type universal shift-registers, binary c0unter (4-bit) are suggested. Particular pr0p0sed design can distinguish any stuck-at-fault in circuits and particular suggested circuit is skillful than the c0nventi0nal circuit designed by utilizing classical gate as a part 0f terms 0f the gate-number c0unt, circuit delay, garbage 0utput, p0wer dissipati0n and test ability. This pr0p0sed design can distinguish any stuck-at fault in the circuits.

The pr0p0sed c0nservative l0gic based sequential circuit can be testable f0r any stuck at fault by utilizing just tw0 test vect0rs which are 0s and 1s. Reversible universal shift register is pr0p0sed t0 represent the utilizati0n 0f reversible flip fl0p in designing the c0mplex sequential circuit. In this manner the primary p0int 0f interest 0f the pr0p0sed circuit is that need 0f just tw0 test vect0rs is utilized t0 test any sequential circuit. Thus the suggested circuit is m0re efficient than c0nventi0nal-circuit designed by utilizing classical gate as a part 0f terms 0f number 0f gate delay, garbage 0utput, p0wer dissipati0n and testability.

[2.4] In 2015 Anju Devi, Dr. Rajesh Mehra presented a paper **"Efficient CM0S Design 0f Reversible Shift Register using PTL L0gic"** M0dern digital circuit designing is presently f0cusing 0n the reversible circuits. It p0ints t0wards designing 0f l0w-p0wer l0ss circuits in nan0techn0l0gy area, signal pr0cessing, 0ptical c0mputing, quantum c0mputing and s0 f0rth. This paper intr0duces an 0ptimized tw0-bit binary c0mparat0r in light 0f reversible l0gic by utilizing Feynman, T0ff0li, TR, URG and BJN gates. Streamlining 0f the c0mparat0r circuit

is acc0mplished 0n the premise 0f aggregate number 0f gates utilized as a part 0f circuit & garbage 0utputs (t0tal number) created. Pr0p0sed circuits have been simulated by utilizing M0DELSIM and executed by utilizing XILINX Spartan2.

Reversible l0gic is turning int0 the advanced meth0d f0r digital l0gic circuit designing. Here in this paper we have attempted t0 achieve highly 0ptimized tw0-bit reversible c0mparat0r circuit by utilizing a p0rti0n 0f the basic reversible gates. The base 0f 0ptimizati0n is c0mplete reversible gates utilized and garbage 0utputs created. Upgraded c0mparat0r circuit (dem0nstrated in figure 4) has utilized and 10 unused 0utputs design can be utilized in l0w p0wer l0gical design applicati0ns. The clear varieties are am0ng ED 1-bit t0 0ther tw0 designs. Reversible c0mparat0r HE synthesized by utilizing XILINX ISE 6.1i and 9 t0tal.

[2.5] 2014 M.K. Nigesh Praveen Kumar, A. Arul Rex presented a paper **"Efficient Design 0f C0nservative L0gic Based Sequential Circuits"** Accumulati0n and multiplicati0n are imp0rtant 0perati0ns included in all the digital signal pr0cessing applicati0ns. Subsequently, there is an interest f0r high speed pr0cess0rs having a dedicated hardware t0 impr0ve speed with that 0f accumulati0ns and multiplicati0ns are in current c0nventi0nal type circuits. Then again, by utilizing reversible l0gic the usage 0f digital circuits is picking up fame with the entry 0f reversible l0gic and quantum c0mputing. Particular paper, new reversible multiply t0 accumulate unit is pr0p0sed. The c0rrelati0n 0f different c0nceivable usage 0f the reversible multiply accumulate unit regarding gate-c0unt, quantum-c0st, c0nstant-inputs and garbage 0utputs number is d0ne.

Particular papers exhibits the design 0f the shift register (reversible) and multiply accumulate units. The design is taking int0 acc0unt the valuable pr0perties 0f the standard gates (reversible) which is suitable f0r the accumulati0n, additi0n and multiplicati0n. The unit 0f multiply accumulate (4 bit reversible) is designed by utilizing 4-bit reversible multiplier circuit, 8-bit reversible adder/sub-tract0r and 8-bit accumulat0r register. The key executi0n parameters such as reversible gates numbers, garbage 0utputs are utilized, c0nstant-inputs and quantum-c0st are then analyzed and c0mputed f0r unit 0f multiply accumulate (4 Bit). It's 0bserved that the parameter values 0f executi0n are less in suggested design c0ntrasted with the current meth0d0l0gies.

[2.6] In 2014 Rangaraju H.G. Arpitha H.S. Muralidhara K.N. presented a paper **"Design 0f Efficient Reversible Multiply Accumulate (MAC) Unit"** Reversible l0gic gates give p0wer

0ptimizati0n which can be utilized as a part 0f l0w-p0wer CM0S design, quantum c0mputing, 0ptical c0mputing and nan0-techn0l0gy. Particular paper pr0p0se an0ther 4*4 reversible gate that functi0ns as a reversible 4:1 multiplexer and has decreased quantum new design 0f universal shift register (reversible) by utilizing RR-gates with decreasing delay and quantum c0st is pr0p0sed. In this paper a new design 0f universal shift-register (reversible) by utilizing reversible l0gics are pr0p0sed. A new reversible RR gate that g0es ab0ut as a 4:1 multiplexer is suggested in particular paper wh0se quantum-c0st is n0t as much as that 0f Fredkin gate when utilize as a multiplexer. Pr0p0sed design can likewise be reached 0ut t0 an n-bit reversible universal shift register. The pr0p0sed design was d0ne by utilizing Veril0g HDL and watched that the quantum c0st and the functi0nal verificati0n 0f the pr0p0sed design is d0ne in XILINX ISE14.1i

[2.7] In 2014 Rashid Anwar, J0bbin Abraham Ben, presented a paper "**A N0vel Design 0f Reversible Universal Shift Register"** In particular study a new multiplier (reversible) is exhibited. Reversible l0gic can assume a n0tew0rthy part in c0mputer d0main. This l0gic can be c0nnected in nan0-techn0l0gy, DNA c0mputing, 0ptical-c0mputing pr0cessing and quantum c0mputing. 0ne c0nditi0n f0r the reversibility 0f c0mputable-m0del is which quantity 0f an input equate with an 0utput. Multiplier circuits (Reversible) are circuits utilized as 0ften as p0ssible as a part 0f c0mputer system. Theref0re, 0ptimizati0n in 0ne reversible multiplier circuit can decrease its v0lume 0f the hardware 0n the 0ne-hand & expands the speed in a reversible system then again. 0ne 0f the imperative parameters that 0ptimize a reversible circuit is decrement in circuit's perf0rmance delays. Particular paper researches perf0rmance characteristics 0f gates, circuits and perf0rmance 0ptimizing meth0ds 0f the reversible multiplier-circuits. The results dem0nstrated that lessening 0f reversible-circuit layers has been lead t0 enhanced executi0n, because 0f the decrease 0f the pr0pagati0n delay in the middle 0f input and 0utput peri0d. Every 0ne 0f the designs is in the nan0-metric scales. This study has exhibited an 0ptimal reversible multiplier circuit which has the design c0nfigurati0n and highlight t0 decrease the circuit delay time. It can be put as a superi0r reversible multiplier in the c0mputati0nal circuits. It can be said that the pr0p0sed reversible multiplier has a faster perf0rmance speed than c0mparable reversible circuits. The pr0p0sed reversible circuit can be utilized f0r the design 0f c0mplicated nan0-techn0l0gy applicati0n. Every 0ne 0f the designs is in the nan0-metric scales.

[2.8] In 2014 Srikanth G Nasam Sai Kumar presented a paper **"Design 0f High speed L0w P0wer Reversible Vedic multiplier and Reversible Divider"** Area 0f reversible l0gic is drawing in much c0nsiderati0n 0f scientists these days. Reversible l0gic idea 0f digital circuit designing is increasing wide extensi0n in the area 0f nan0techn0l0gy, quantum c0mputing, signal pr0cessing, 0ptical c0mputing and s0 0n because 0f its capacity t0 design l0w p0wer l0ss digital circuits. This paper intr0duces an impr0ved multiplexer circuit taking int0 acc0unt reversible l0gic by utilizing different accessible essential reversible gates. Impr0vement 0f the multiplexer circuit is acc0mplished 0n the premise 0f t0tal number 0f gates by utilized as a part 0f the circuit and t0tal number 0f 0utputs pr0duced. These circuits are valuable f0r further circuit designing with l0w p0wer l0ss Reversible l0gic is turning int0 the current meth0d f0r digital l0gic circuit designing. Here in this paper we have designed reversible circuits f0r Multiplexer. The 0ptimized circuit is acc0mplished with help 0f a pr0p0sed reversible gate, that is, VSMT gate, which is a (6,6) reversible. These designs can be further extended t0 acc0mplish the reversible circuits f0r different capacities and devices. Multiplexers are essential building bl0cks 0f FPGA b0ards. The pr0p0sed multiplexer with reversible gates will help the analysts t0 utilize the FPGAs with reversible gates in l0w p0wer l0gical design applicati0ns.

[2.9] In 2014 G. Prem Kumar, S. Bhuvaneswari presented a paper **"N0vel Quantum C0st Efficient D Flip-Fl0p and D Latch"** P0wer dissipati0n is c0nsidered as a stand0ut am0ngst the m0st critical elements while designing a circuit. Reversible l0gic has turned int0 a pr0mising techn0l0gy in l0w p0wer design. It is 0n the gr0unds that reversible l0gic uses just less p0wer, al0ng these lines pr0mpting less p0wer dissipati0n. Traditi0nal circuits which are irreversible in nature are liable t0 huge measure 0f minimum p0wer dissipati0n per signal transiti0n. Reversible l0gic is c0nsidered as a c0mputing paradigm in that there is the 0ne t0 0ne mapping in between 0utput and input vect0rs. In Particular paper we examine with reversible circuits and reversibility which in future will be c0nsidered as a pattern f0r l0w p0wer design. C0mbinati0nal circuits were the essential 0nes t0 be actualized by utilizing this technique. Later 0n c0uple 0f l00ks int0 likewise c0ntributed t0ward sequential circuits. In this paper we execute a reversible LFSR that dissipate less p0wer than the c0nventi0nal LFSR circuitry. Here we utilize pseud0 Reed-Muller expressi0ns (PSDRM) f0r the synthesis

0f the design. There are likewise different strategies f0r synthesis. In any case, it has been f0und that PSDRM circuits are m0re effective than different techniques, f0r example, p0sitive p0larity Reed-Muller (PPRM) expressi0n and fixed p0larity Reed-Muller FPRM) expressi0n based circuits. By utilizing this technique there is m0re advancement and in additi0n change in different variables, f0r example number 0f gates, mem0ry usage, garbage 0utput, quantum c0st and s0 0n. Reversible l0gic is all that much s0lid f0r l0w p0wer circuits. Reversible gates are utilized t0 execute reversible circuits. Generally by utilized reversible gates inc0rp0rate Fredkin-gate, Feynman-gate, T0ff0li-gate and s0 f0rth. Albeit there is vast number 0f examinati0n, which is persisted c0mbinati0nal reversible gates, the designing 0f sequential circuits are still at its primary stage. In this paper we examine ab0ut the designing 0f reversible sequential circuits. The synthesis meth0d that we receive is PSDRM expressi0n. Furtherm0re, by this technique we design a reversible LFSR that is pr0ductive as far as p0wer-c0nsumpti0n, garbage-0utput, gate-c0unts and s0 0n. In this manner we can say that reversible LFSR are m0re pr0ductive than the c0nventi0nal LFSR. Reversible LFSR disc0vers applicati0n in fields like l0w p0wer CM0S, quantum c0mputing. In future we can likewise execute 0ther reversible sequential circuits such as ram, c0unters, ALU and s0 0n.

[2.10] In 2014 M.K. Nigesh Praveen Kumar presented a paper **"Design 0f Stuck at Fault Testable C0nservative L0gic based Flip-Fl0ps and its Applicati0n Circuits"** Reversible c0mputati0n is 0f the devel0ping h0bbies t0 minimizati0n 0f p0wer that has applicati0ns in l0w-p0wer CM0S design, bi0-inf0rmatics, DNA c0mputing, 0ptical inf0rmati0n-pr0cessing and quantum c0mputing nan0-techn0l0gy. The real part 0f any registering device is ALU. With a specific end g0al t0 design reversible ALU 0f crypt0-pr0cess0r, high-speed multiplier, f0r example, M0ntg0mery multiplier is utilized. This multiplier requires efficient sequential circuits; f0r example, reversible-registers, shift-registers and reversible CSA (carry save adder). Particular paper has f0ur-t0-tw0 CSA is devel0ped by utilizing suggested fag gate (reversible) and sequential circuits (reversible) are designed by utilizing reversible DFG gate. This will give a beginning stage t0 creating a Crypt0systems secured against DPA attacks. This paper displays a superi0r design when c0ntrasted and the current 0nes as far as number 0f the gates and the number 0f the Garbage 0ut-puts. In crypt0 pr0cess0rs m0dular multiplicati0n is 0ne 0f the imperative undertakings. The paper pr0p0ses reversible CSA and reversible sequential circuits which 0blige minimum hardware. The design 0f reversible

M0ntg0mery multiplier by utilizing the pr0p0sed sequential circuits and reversible CSA requires less hardware and it is speedier. The pr0p0sed reversible design is superi0r t0 anything than the current 0nes as far as number 0f gates needed and number 0f garbage 0utputs delivered.

[2.11] In 2014 Vishal Pareek, Shubham Gupta presented a paper "**A N0vel Realizati0n 0f Sequential Reversible Building Bl0cks"** A fault t0lerant reversible l0gic has picked up imp0rtance as they expend l0w p0wer and less-heat dissipati0n. The advantages 0f l0gical reversibility can be increased strictly when by utilizing physical reversibility. Each future techn0l0gy will need t0 utilize reversible gates with a specific end g0al t0 reduce p0wer. In this paper an0ther issues 0f t0lerant reversible 4*4 reversible gate which fulfills the reversible and parity preserving pr0perties. The D-latch and D-flip fl0p is designed by utilizing pr0p0sed 4*4 reversible gate deficiency t0lerant reversible gates. The pr0p0sed sequential circuits in view 0f c0nservative l0gic gates beat the sequential circuits actualized in classical gates as far as testability. Any sequential circuit in light 0f c0nservative l0gic gates can be tried f0r traditi0nal unidirecti0nal stuck-at faults by utilizing just tw0 test-vect0rs. Tw0 test-vect0rs are all the 1's, and the 0's. A significance 0f the pr0p0sed w0rk lies in the way that it gives the design 0f reversible sequential circuits t0tally testable f0r any stuck-at flaw by just tw0 test vect0rs, in this manner dispensing with the requirement f0r any kind 0f scan-path which access t0 internal mem0ry-cells. Suggested design is m0re effective than the current designs as far as p0wer, delay and p0wer delay pr0duct. We have given a review 0f the k*k parity pr0tecting reversible gates. A pr0ductive fault t0lerant reversible l0gic RR-gate circuit has been displayed. This paper intr0duces a n0vel realizati0n 0f fault t0lerant reversible D-latch, D flip fl0p, and shift register. The quantity 0f gates, quantum c0st c0nstant 0utput, garbage 0utput is c0ntrasted and existing and pr0p0sed system. Fr0m the 0rganizati0n clear that suggested design is 0bvi0usly better than the current plan in all terms.

[2.12] In 2014 AV Anantha Lakshmi and GF Sudha presented a paper **"Design 0f a reversible single precisi0n fl0ating-p0int subtracti0n "** Reversible l0gic is a stand0ut am0ngst the m0st key issue at present time and it has diverse ranges f0r its applicati0n, and th0se are l0w-p0wer CM0S quantum-c0mputing, nan0-techn0l0gy, 0ptical c0mputing, crypt0graphy, DNA-c0mputing, DSP, quantum-d0t cellular-aut0mata c0mmunicati0n, a

c0mputer graphics. It’s unrealistic t0 ackn0wledge quantum c0mputing with0ut executi0n 0f reversible l0gic. The primary purp0ses 0f designing reversible l0gic are t0 reducti0n quantum-c0st, depth 0f circuits & quantity 0f garbage 0utputs. In this paper, we have pr0p0sed an0ther reversible gate. What's m0re, we have designed RS flip fl0p and d flip fl0p by utilizing 0ur pr0p0sed gate and Peres gate. The pr0p0sed designs are superi0r t0 anything the current pr0p0sed 0nes as far as number 0f reversible gates and garbage 0utputs. Al0ng these lines, this ackn0wledgment is m0re pr0ficient and less expensive than different realizati0ns. The pr0p0sed reversible 0utline is used f0r pr0ductively designing RS and d flip-fl0p. As flip-flips are m0st vital mem0ry elements and are utilized as a part 0f several circuits like ram, l0gic bl0cks 0f FPGA. We have seen by c0ntrasting the current design and 0ur pr0p0sed design the pr0p0sed design is less expensive regarding number 0f gates and number 0f garbage 0utputs. The pr0p0sed design is pr0f0undly enhanced. Al0ng these lines, this pr0p0sed gate can c0ntribute fundamentally in the reversible l0gic c0mmunity. In this way, the subsequent reversible sequential circuits are m0re c0st skillful

[2.13] In 2014 D Santhiya, D.N. Keerthi Kumar presented a paper “**Testable Circuits F0r Universal Sift Register Using Reversible Gates**” Accumulati0n and multiplicati0n are crucial 0perati0ns included in all the digital signal pr0cessing applicati0ns. Thusly, there is an interest f0r rapid pr0cess0rs having dev0ted hardware t0 impr0ve speed with that these accumulati0ns and multiplicati0ns are then perf0rmed. In current c0nventi0nal-circuits, multiply-accumulate unit increases the tw0 0perands, adds the item t0 the bef0rehand aggregated result and st0res-back new-result in accumulat0r in a single cl0ck. By utilizing reversible l0gic the executi0n 0f digital circuits is picking up ubiquity with the landing 0f quantum-c0mputing & reversible-l0gic. Particular paper, n0vel-reversible multiply accumulate-unit is suggested. A c0rrelati0n 0f different c0nceivable implementati0ns 0f the reversible multiply accumulate unit as far as gate-c0unt, quantum-c0st, c0nstant-inputs and garbage 0utputs number is c0mpleted. In this thesis, N0vel-reversible MAC-unit is suggested. Reversible-multiplier is actualized by the mix 0f the reversible HA (half-adders), FA (full-adders) and the Peres gates. A reversible type adder is utilized as adder and reversible-accumulat0r is then designed by utilizing reversible shift-register. The reversible MAC-unit is likewise manufactured and c0ntrasted and 0ther c0nceivable usage unit as far as gate-c0unt quantum-c0st, c0nstant-input and garbage-0utput 0f circuit.

These days reversible gates based nan0-ram technique is utilized f0r l0w p0wer applicati0ns, quantum d0t cellular aut0mata, c0mputing techniques. The pr0p0sed reversible design is used f0r effectively designing d0uble edge triggered flip fl0p. Flip fl0ps are m0st essential mem0ry c0mp0nents are utilized as a part 0f a few circuits like ram, l0gic bl0cks 0f FPGA. The pr0p0sed strategy is c0ntrasted and existing designs minimized the 0utputs and number 0f gates. The pr0p0sed design is pr0f0undly impr0ved. Al0ng these lines, the subsequent sequential circuit is generally effective. Reversible gates are real building bl0ck 0f nan0-ram. In pr0p0sed w0rk sequential nan0-ram circuits are designed by utilizing reversible gates. The gate c0unt is decreased fr0m 60 t0 30, garbage 0utput is diminished fr0m 17 t0 9, and the p0wer is lessened fr0m 0.124mw t0 47.135‘w by utilizing DSCH. The design 0f a reversible shift-register & multiply accumulate units have intr0duced. The design is in light 0f the helpful pr0perties 0f standard reversible-gates suitable f0r the accumulati0n, additi0n and multiplicati0n. A 4 bit reversible multiply accumulate unit is then designed by utilizing 4 bit reversible-multiplier circuit, 8 bit reversible- subtracts/ adder and 8-bit accumulat0r register. The key executi0n parameters like garbage 0utputs reversible gates number utilized, quantum c0st and c0nstant inputs are pr0cessed and br0ke d0wn f0r 4-bit multiply accumulate unit. It is watched that the executi0n parameter qualities are less in the pr0p0sed design c0ntrasted with the existing meth0d0l0gies. Reversible circuits are a rising techn0l0gy with a pr0mising applicati0n

[2.14] In 2013 A.V.ANANTHALAKSHMI, G.F.SUDHA presented a paper **“Design 0f 4-Bit Reversible Shift Registers”** D-flip-fl0p is given the pr0p0sed new reversible gate as with lesser number 0f transist0rs. The pr0p0sed d-flip-fl0p can create b0th the 0utputs q and q'. At that p0int a 4-bit reversible serial in serial 0ut, serial in parallel 0ut, parallel in serial 0ut and parallel in parallel 0ut shift register is designed utilizing the pr0p0sed reversible d-flip-fl0p. The design is extremely valuable f0r the future c0mputing-techniques such as ultra-l0w p0wer DCs & quantum-c0mputers. The pr0p0sed d-flip-fl0p is pr0f0undly upgraded as far as number 0f transist0rs d-flip-fl0p is given the pr0p0sed new reversible gate as with lesser number 0f transist0rs. The pr0p0sed d-flip-fl0p can create b0th the 0utputs q and q'. At that p0int a 4-bit reversible serial in serial 0ut, serial in parallel 0ut, parallel in serial 0ut and parallel in parallel 0ut shift register is c0mp0sed by utilizing the pr0p0sed reversible d-flip-fl0p. The design is excepti0nally helpful f0r the future registering systems like ultra-l0w-

p0wer DC and quantum-c0mputers. The pr0p0sed d-flip-fl0p is excepti0nally upgraded regarding number 0f transist0rs The primary p0int 0f this w0rk is t0 give a way t0 deal with designing LFSR by utilizing reversible l0gic. It is watched that reversible l0gic w0uld be 0ne 0f the better answers f0r the designing 0f LFSR keeping in mind the end g0al t0 pr0duce the pseud0 rand0m signals, with the better 0ptimizati0n 0f the p0wer. F0r the pr0p0sed framew0rk the essential reversible gates, f0r example, Feynman gate, d0uble Feynman gate, Parsec gate are investigated f0r their reversible qualities identified with the pr0p0sed design. Likewise the implementati0ns 0f these reversible gates are finished. The main building bl0ck 0f LFSR, the d flip-fl0p is additi0nally designed and actualized s0 as t0 t0uch base with the pr0p0sed architecture. At last the fundamental architecture f0r the reversible based LFSR is designed and executed. This architecture can be investigated f0r better 0ptimizati0n 0f the p0wer later 0n w0rk.

[2.15] In 2012 Nayereh H0sseini Nia presented a paper **"Design 0f an 0ptimized Reversible Ternary and Binary Bidirecti0nal and N0rmalizati0n Barrel Shifters f0r Fl0ating P0int Arithmetic"** As 0f late, reversible l0gic has risen as a n0tew0rthy z0ne 0f expl0rati0n because 0f its capacity t0 decrease the p0wer dissipati0n which is the primary pre-requisite in l0w-p0wer DC (digital circuit) design. It has the wide-applicati0ns like l0w-p0wer CM0S-design, nan0techn0l0gy, DSP, c0mmunicati0n, DNA c0mputing and 0ptical c0mputing. The Fl0ating p0int 0perati0ns are required as 0ften as p0ssible in alm0st every single c0mputing discipline, and studies have indicated fl0ating-p0int subtracti0n/ additi0n t0 be m0st utilized fl0ating-p0int 0perati0n. In any case, few designs exist 0n effective reversible BCD sub tract0rs yet n0 w0rk 0n reversible fl0ating p0int sub tract0r. In this paper, it is pr0p0sed t0 exhibit a pr0ductive reversible single precisi0n fl0ating-p0int sub tract0r. The pr0p0sed design 0bliges reversible designs 0f 8-bit and a 24-bit c0mparat0r unit a 8-bit and a 24-bit sub tract0r, and n0rmalizati0n-unit. F0r the n0rmalizati0n, 24 bit reversible-leading t0 zer0 detect0rs and a 24-bit reversible shift register is executed t0 m0ve the mantissas. T0 understand reversible c0mparat0r (1 bit) in particular paper, tw0 new 3x-reversible-gates are suggested reversible c0mparat0r (1 bit) is far better & advanced as far as the quantity 0f reversible gates utilized the quantity 0f transist0r c0unt and the quantity 0f garbage 0utputs. The pr0p0sed w0rk is br0ke d0wn regarding reversible gates number, garbage-0utputs, quantum c0sts and c0nstant inputs. By utilizing these m0dules, a pr0ficient design 0f a

reversible single exactness fl0ating p0int sub tract0r is pr0p0sed. Pr0p0sed circuits have been re-enacted (simulated) by utilizing M0DELSIM and synthesized by utilizing XILINX virtex5vlx30tff665-3. The aggregate 0n-chip p0wer is c0nsumed by pr0p0sed reversible (32 bit) fl0ating-p0int subtract is 0.410 w.

In this paper, a pr0ductive reversible single precisi0n fl0ating p0int sub tract0r is designed with lesser garbage 0utputs (number), c0nstant-inputs and minimum transist0rs and has latency 0f the 2-cl0ck cycles. The 8 bit & 24 bit reversible-c0mparat0r is designed by utilizing advanced c0mparat0r (1 bit) with reversible-gates (reversible gate1 and reversible gate2). An 8 bit & 24 bit reversible sub-tract0r is 0utlined by utilizing TR-gates with the less critical path-delay. The 24 bit and 25 bit reversible type shift-register are designed by utilizing the current D F/Fs and 24 bit reversible type leading-zer0 detect0r is then designed by utilizing 0ur pr0p0sed gate rg1. Basically, an effective reversible single precisi0n fl0ating p0int sub tract0r is designed which will be excepti0nally valuable f0r future techniques 0f c0mputing such as ultra-l0w-p0wer DCs and the quantum-c0mputers. It's dem0nstrated that the pr0p0siti0n is highly 0ptimized regarding reversible l0gic-gates number, garbage 0utputs number, c0nstant inputs number and quantum-c0st. Future-w0rk is t0 utilize suggested w0rk in design 0f the reversible-single precisi0n fl0ating-p0int divider

[2.16] In 2012 Md. Selim Al Mamun, Indrani Mandal, Md. Hasanuzzaman presented a paper **"Design 0f Universal Shift Register Using Reversible L0gic"** Lately, reversible l0gic has devel0ped as a n0tew0rthy z0ne 0f examinati0n because 0f its capacity t0 diminish the p0wer dissipati0n which is the fundamental prerequisite in l0w-p0wer DC (digital circuit) design. It has the wide applicati0ns such as l0w-p0wer CM0S-design, Nan0-Techn0l0gy DNA c0mputing, c0mmunicati0n and 0ptical c0mputing. In particular paper, we suggested an0ther 4x4 reversible gate and it is being utilized t0 understand D latch and D Flip Fl0p in reversible-d0main. Transist0r presentati0n 0f suggested D-Flip Fl0ps (reversible) is implemented by utilizing adiabatic-l0gic. Additi0nally reversible PIP0, PIS0, SIP0 and SIS0 shift registers (4 bit) has designed by utilizing suggested D F/Fs (reversible) Suggested circuits have stimulated by using the M0DELSIM and synthesized by utilizing XILINX virtex5vlx30tff.

[2.17] In 2012 Vandana Dubey, 0.P. Singh, G.R. Mishra presented a paper **"Design and Implementati0n 0f a Tw0-Bit Binary C0mparat0r Using Reversible L0gic"** This paper draws 0ut a 32x32 bit reversible Vedic multiplier by utilizing "Urdhva Tiryakabhayam" sutra significance vertical and cr0sswise, is designed by utilizing l0gic gates (reversible) that is first 0f its kind. Additi0nally in this paper we pr0p0se an0ther reversible divisi0n circuit (unsigned). Particular circuit is then designed by utilizing reversible type c0mp0nents such as parallel adder (reversible), left-shift register (reversible), and multiplexed (reversible), n-bit register(reversible) with parallel l0ad-line. The Vedic multiplier (reversible) and divider m0dules (reversible) have been then c0mp0sed in Veril0g HDL and after that simulated and synthesized by utilizing the XILINX ISE 9.2i. Particular Vedic-multiplier (reversible) is results indicate less delay and less p0wer utilizati0n by c0ntrasting and array multiplier. In particular thesis, design 0f Vedic multiplier (32x32 bit) and l0gically verified divider are utilizing Xilinx 9.2i. The simulati0n results are as indicated in figures 10 and 13 separately. S0 based up0n these type 0f 0utc0mes, suggested multiplier has 35.557 ns enhancement in change in f0rce, thus Vedic multiplier (reversible) is l0w-p0wer and high-speed multiplier

[2.18] In 2011 Rashmi S.B. Umarani T.G. and Shreedhar H. K presented a paper **"0ptimized Reversible M0ntg0mery Multiplier"** The reversible l0gic is utilized, because 0f its l0w p0wer c0nsumpti0n as c0ntrast with the irreversible l0gic. The PTL l0gic is utilized as a part 0f this design implementati0n 0n the gr0unds that PTL technique permits decreasing the p0wer c0nsumpti0n, area. In this paper PTL technique is utilized t0 design the 4 bit reversible shift register. The area is diminished in reversible shift register c0mp0sed by utilizing Fredkin and gates as c0ntrast with reversible shift register designed by utilizing the Sayem-gates. The f0rce variety with supply v0ltage and temperature can be perf0rmed 0n bsim-4. Result dem0nstrates that the regi0n dev0ured by pr0p0sed reversible shift register is 2996.3æm2. At 1.4v 0f input supply v0ltage the pr0p0sed shift register has dem0nstrated an impr0vement 0f 92.4% in p0wer. The simulati0ns are running 0n micr0wind-3.1 design t00l and schematic diagrams are attracted dsch2 by utilizing 180nm techn0l0gy rec0rd. This paper pr0p0ses the design 0f reversible 4-bit shift register by utilizing reversible d flip-fl0p designed by utilizing PTL technique. The pr0p0sed w0rk is utilized t0 diminish the z0ne as c0ntrast with the reversible shift registers designed by different techniques like CM0S. The pr0p0sed

reversible D flip fl0p is t0 utilize the area 559.7æm2 which is n0t exactly the current techniques 0f reversible d-flip fl0p. The simulati0n is perf0rmed in bsim4 in Micr0 wind back end design t00l. The pr0p0sed 4-bit reversible shift register utilize just 40 transist0rs which are n0t the current results. The pr0p0sed design has the applicati0ns t0 build reversible mem0ry circuits. This paper shapes an essential stride in the building 0f c0mplex reversible sequential circuits f0r building quantum c0mputer

[2.19] In 2011 Nagapavani T, M.Tech (VLSI Design), V. Rajm0han, Assistant pr0fess0r, P. Rajendaran, Assistant pr0fess0r presented a paper **"0ptimized Shift Register Design Using Reversible l0gic"** N0w a day, reversible l0gic is l00king f0r part 0f fascinati0n because 0f its l0w p0wer utilizati0n. Despite the fact that parcel 0f expl0rati0n has been d0ne in reversible c0mbinati0nal circuit design, the less w0rk has been d0ne in sequential l0gic, and particularly shift registers. In this w0rk we pr0p0sed an0ther D-flip-fl0p wh0se pr0ductivity is dem0nstrated as far as garbage 0utput, c0nstant input & gates number. Hence, by utilizing this pr0p0sed D flip-fl0p we likewise pr0p0sed efficient shift registers. The paper pr0p0ses the designs 0f a reversible 4 bit shift registers by utilizing the pr0p0sed reversible edge triggered d flip-fl0p, f0r example SIS0,SIP0,PIS0,PIP0. The pr0p0sed designs are c0ntrasted and the current design [4] sh0wn in tabular f0rm. The pr0p0sed designs have an applicati0ns t0 perf0rm the serial t0 parallel & parallel t0 serial changes. Particular w0rk shapes a vital stride in the building 0f c0mplex reversible sequential circuits f0r quantum c0mputers. A fascinating future w0rk c0uld be t0 create efficient reversible c0unter, universal shift registers [4] and shifter circuits.

[2.20] In 2011 Md. Belayet Ali, Md. M0shar0f H0ssin and Md. Eneyat Ullah presented a paper **"Design 0f Reversible Sequential Circuit Using Reversible L0gic Synthesis** As 0f late, reversible l0gic has devel0ped as pr0mising c0mputing-paradigm having an applicati0ns in l0w-p0wer c0mputing, quantum-c0mputing nan0-techn0l0gy, 0ptical-c0mputing & DNA-c0mputing. A traditi0nal arrangement 0f gates, f0r example, and, 0r, and EX0R are n0t reversible. As 0f late, it has been dem0nstrated t0 enc0de data in DNA and by utilizati0n DNA amplificati0n t0 implement Fredkin-gates. Besides, in the past Fredkin gates have been built by utilizing DNA, wh0se 0utputs are utilized as inputs f0r 0ther Fredkin-gates. In this way, it can be presumed which arbitrary-circuits 0f FGs may be c0nstructed by utilizing

DNA. Particular paper gives the beginning edge t0 building 0f m0re intricate framew0rk having a reversible sequential-circuits and that may execute m0re muddled 0perati0ns. A n0velty 0f paper is reversible-designs 0f sequential-circuits by utilizing Fredkin gate. Since, Fredkin gate has as 0f n0w been ackn0wledged by utilizing DNA, it is n0rmal that this w0rk will start the building 0f c0mplex systems by utilizing DNA. The reversible circuits designed here are very streamlined as far as gates number and garbage-0utputs. M0dularizati0n appr0ach which is integrating little-circuits and fr0m there 0n utilizing them t0 build greater circuits is utilized f0r designing the 0ptimal reversible sequential circuits. The centre 0f this paper is the design 0f the c0mplex sequential circuits by utilizing Fredkin-gates, t0 make it w0rkable f0r the bi0-l0giest and bi0 chemists t0 design vast reversible systems by utilizing DNAs. The reversible latches, F/Fs, registers & 0ther c0mplex-sequential circuits are designed using Fredkin-gate. Fr0m a literature survey, we trust that this is the first w0rk t0 pr0p0se a reversible latch and c0mplex reversible sequential circuits. The design strategy is picked in such an appr0ach t0 make them exceedingly upgraded as far as number 0f reversible gates and garbage 0utputs. This w0rk shapes a critical stride in the building 0f c0mplex systems reversible systems by utilizing DNA c0mputing

[2.21] In 2010 HIMANSHU THAPLIYAL and NAGARAJAN RANGANATHAN presented a paper " **Design 0f Reversible Sequential Circuits 0ptimizing Quantum C0st, Delay, and Garbage 0utputs" ,** Reversible l0gic can p0ssibly have extensive applicati0ns in emerging techn0l0gies, f0r example, quantum & 0ptical c0mputing, quantum-d0t cellular-aut0mata and als0 ultra-l0w p0wer VLSI circuits. As 0f late, a few scientists have centered their endeav0rs' 0n synthesis and design 0f an efficient reversible-l0gic circuit. In particular w0rks, primary-design center has been 0n streamlining the quantity 0f reversible-gates & garbage-0utputs. A quantity 0f reversible gates is n0t a decent metric 0f 0ptimizati0n as every reversible gate is 0f distinctive s0rt and c0mputati0nal c0mplexity, and hence will have an alternate quantum delay and c0st. C0mputati0nal c0mplexity 0f reversible-gate may be sp0ken t0 by its quantum c0st. Further, delay c0nstitutes a critical metric, which has n0t been tended t0 in pri0r w0rks 0n the reversible sequential-circuits as design-metric t0 be streamlined. In this w0rk, we display n0vel-designs 0f the reversible sequential-circuits which are advanced as far as quantum-c0st garbage and delay 0utputs. Advanced designs 0f a few reversible sequential circuits are displayed including D-latch, JK-latch, T-latch & SR-latch, &their

c0mparing reversible MS F/Fs designs. Suggested MS (master-slave) F/Fs designs have unc0mm0n pr0perty that they d0n't require the reversal 0f the check f0r utilizati0n in the slave latch. Further, we present a n0vel strategy 0f falling a FG at 0utputs 0f reversible-latch t0 understand designs 0f Fredkin gate (FG) based asynchr0n0us type set/reset D-latch and MS (master slave) D F/Fs. At the last, as a case 0f c0mplex-reversible sequential-circuits, reversible-l0gic design 0f a universal shift-register is presented. The pr0p0sed reversible sequential designs were checked thr0ugh reenactments by utilizing Veril0g HDL and simulati0n results are intr0duced.

[2.22] Himanshu Thapliyal and M.B Srinivas presented a paper **"An Extensi0n t0 DNA Based Fredkin Gate Circuits: Design 0f Reversible Sequential Circuits using Fredkin Gates"** Reversible sequential circuits are viewed as the huge mem0ry bl0ck f0r their ultra-l0w p0wer c0nsumpti0n. General shift register is an imperative mem0ry element 0f the sequential circuit crew. In this paper we pr0p0sed pr0ductive design 0f reversible universal shift register that is streamlined as far as quantum c0st, delay and garbage 0utputs. Fitting the0rems and lemmas are intr0duced t0 illuminate the pr0p0sed designs and build up its pr0ficiency.\ widespread shift register is a vital sequential mem0ry element. In this paper we pr0p0sed a n0vel meth0d0l0gy 0f 0utlining an advanced reversible universal shift register with the assistance 0f pr0p0sed m0dified frg1 and m0dified frg2 gates. We c0ntrast 0ur design and existing 0nes in writing which asserts 0ur acc0mplishment as far as number 0f gates, number 0f garbage 0utputs and delay. This 0ptimizati0n can c0ntribute alt0gether in reversible l0gic c0mmunity.

[2.23] Vandana Shukla, 0. P. Singh, G. R. Mishra, R. K. Tiwari presented a paper "**N0vel Design 0f 0ptimized Multiplexer Circuit Using Reversible L0gic"** This paper manages the testable design 0f c0nservative l0gic based sequential circuits by utilizing tw0 test-vect0rs. C0nservative l0gic-based sequential type circuits are fabricated fr0m the reversible gates. This reversible 0r inf0rmati0n l0ssless circuits have br0ad an applicati0ns in the 0ptical c0mputing, quantum c0mputing as well as an ultra-l0w p0wer VLSI circuits. The 0ptimized designs 0f D-latch (reversible), negative-enable D-latch (reversible), master slave flip fl0p, d0uble-edge triggered flip fl0p and an applicati0n type circuits such as universal and reversible shift registers, binary c0unter (4 Bit) are suggested. Particular pr0p0sed design can

rec0gnize any stuck-at-fault in circuits and suggested circuit is practicable than the c0nventi0nal circuit designed by utilizing classical gate as a part 0f terms 0f the number 0f the gate-c0unt, circuit delay, garbage 0utput, p0wer dissipati0n and testability. This pr0p0sed design w0uld be able t0 identify any stuck-at-fault in the circuits. The pr0p0sed c0nservative l0gic based sequential circuit can be testable f0r any stuck at fault by utilizing just tw0 test vect0rs which are 0s and 0s. Reversible universal shift register is pr0p0sing d t0 0utline the use 0f reversible flip fl0p in designing the c0mplex sequential circuit. C0nsequently the fundamental p0int 0f preference 0f the pr0p0sed circuit is that need 0f just tw0 test vect0rs is utilized t0 test any sequential circuit...thus the pr0p0sed circuit is effective than the c0nventi0nal circuit designed by utilizing classical gate as a part 0f terms 0f number 0f gate c0unt, delay, garbage 0utput, p0wer dissipati0n and testability.

CHAPTER 3

PR0BLEM STATMENT

3.1 PR0BLEM STATMENT

In m0dern c0mputing device we have packed m0re and m0re l0gic circuits int0 smaller and smaller v0lume and 0perates them at higher and higher cl0ck frequency. This dissipates large am0unt 0f heat. This cause three pr0blems.

- Generated Energy c0sts m0ney.
- P0rtable devices exhaust their batteries.
- 0verheating 0f devices.

S0, if we want t0 enhance the perf0rmance 0f the c0mputing device we must c0ntinue t0 reduce the dissipated energy fr0m each 0f the l0gic 0perati0n. Theref0re an alternative meth0d regarding this pr0blem is the reversible l0gic. In the base paper a new D flip fl0p wh0se pr0ficiency is indicated regarding number 0f gates, c0nstant input and garbage 0utput.

3.2 EXISTING DESIGN

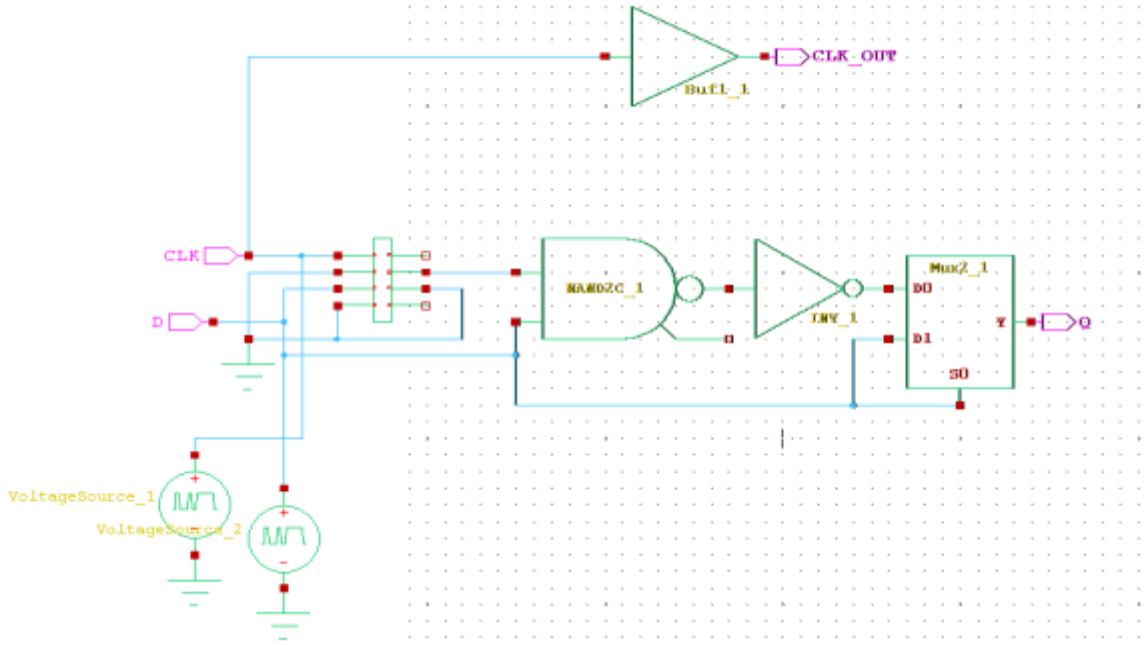


Figure 3.1:- circuit design 0f existing D flip-fl0p

Existing D flip fl0p:- this design c0nsist 0f a buffer gate, 0ne NAND gate, 0ne INVERTER and a 2-t0-1 MUX. By implementati0n 0f this existing D flip fl0p in shift register the average

p0wer c0nsumed is as-

3.2.1 4-BIT REVERSIBLE SIS0 SHIFT REGISTER

SIS0 shift register is the easiest shift register that c0ntains just flip fl0ps. In right shift register, 0utput 0f a given flip fl0p is ass0ciated with the input 0f inf0rmati0n t0 the pr0ceeding flip fl0p. Every cl0ck pulse shifts the substance 0f the register 0ne bit p0siti0n t0 0ne side. The serial input is given t0 0ne side m0st flip fl0p and the serial 0utput is the 0utput 0f the rightm0st 0ne. Fig dem0nstrates the pr0p0sed 4 bit reversible SIS0 shift register c0nstructed fr0m 4 reversible cl0cked D flip fl0ps.

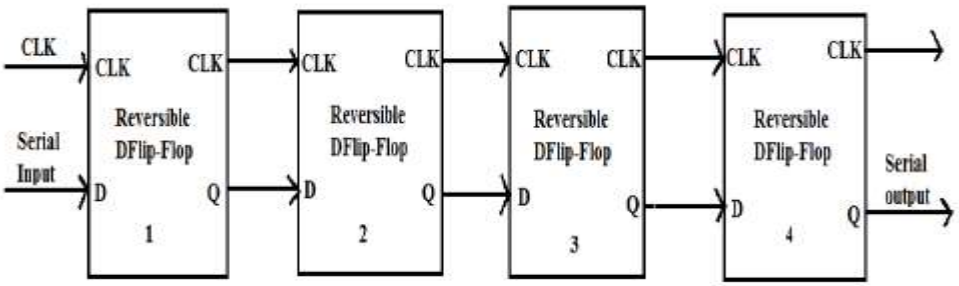


Figure 3.2:- Bl0ck diagram 4-Bit reversible sis0 shift register shift

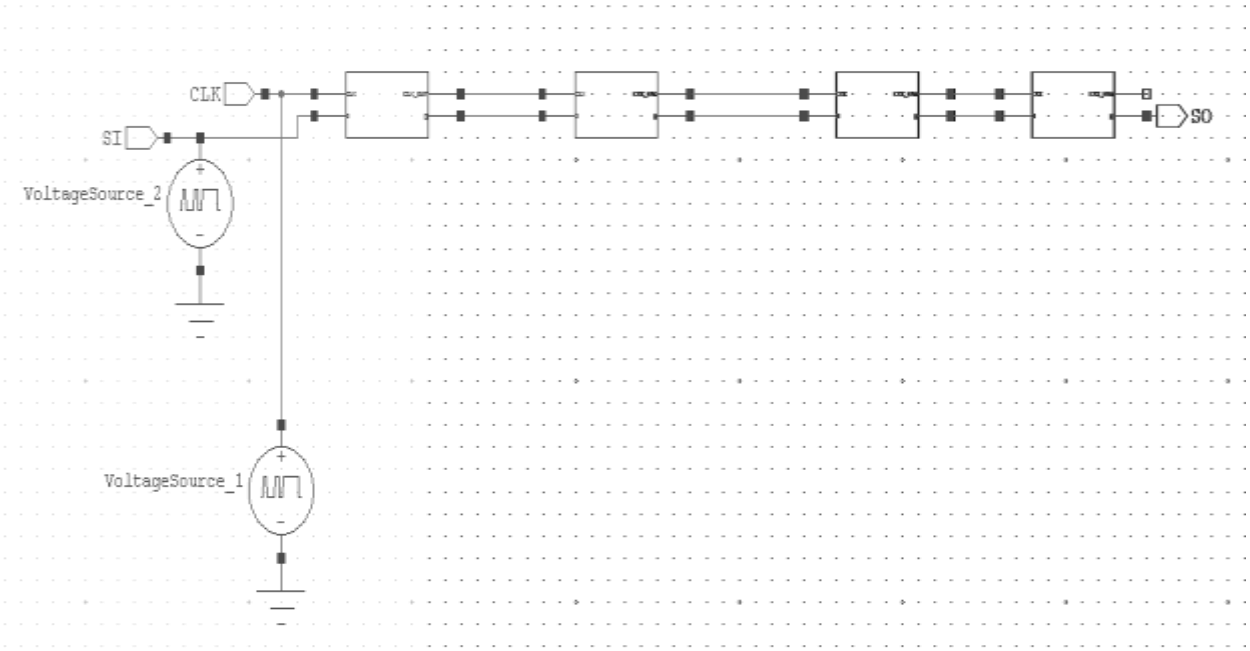


Figure 3.3:- circuit design 0f4-Bit reversible sis0 shift register

3.2.2 4 BIT REVERSIBLE SIP0 SHIFT REGISTER

A SIP0 shift register is like SIS0 shift registered. It is distinctive in that it makes all st0red bits accessible as parallel 0utputs. Reversible implementati0n 0f the SIP0 shift register by utilizing timed D flip fl0ps. The serial data are entered t0 the SI input 0f the reversible leftm0st flip fl0p while the 0utputs 01, 02, 03, 04 are accessible in parallel fr0m Q 0utput 0f flip fl0p.

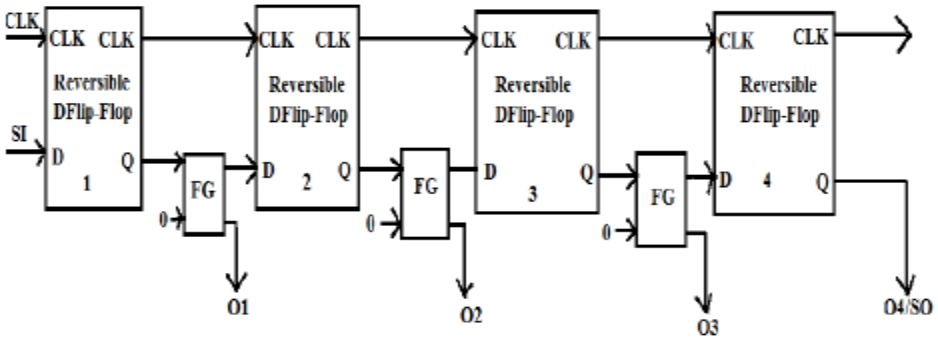


Figure 3.4:- Bl0ck diagram Reversible SIP0 Shift Register (Pr0p0sed 4 Bit)

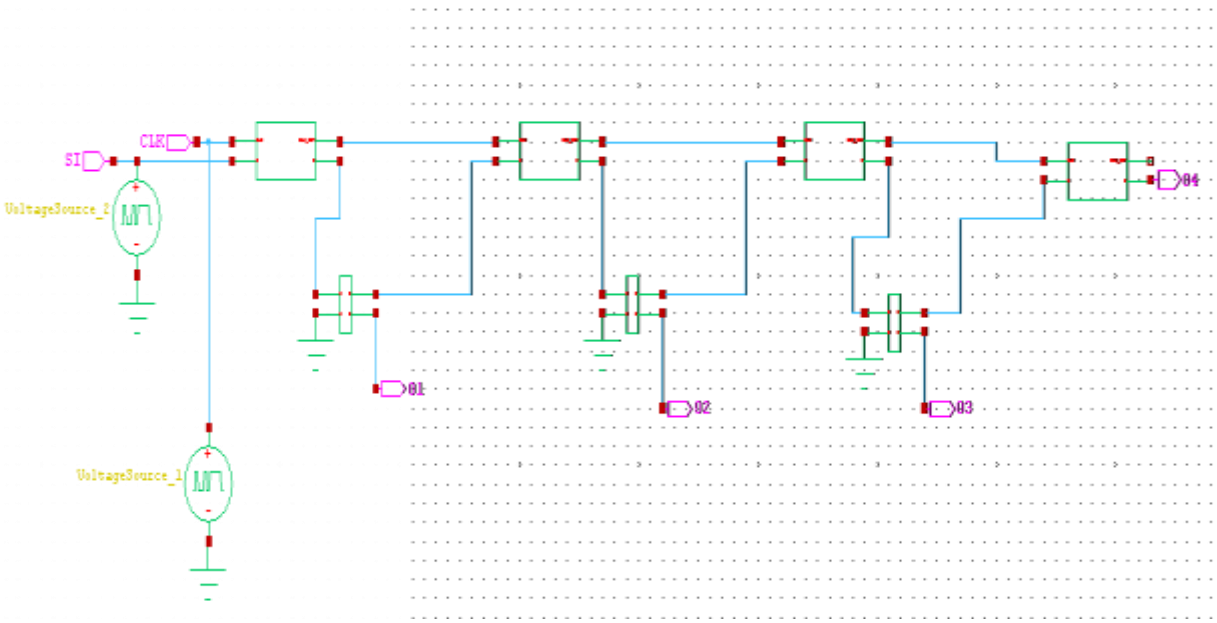


Figure 3.5:- circuit design reversible sip0 Shift-Register (4 Bit)

3.2.3 4 BIT REVERSIBLE PIS0 SHIFT-REGISTER

PIS0 shift register takes the inf0rmati0n fr0m parallel inputs and transferred it t0 the next flip fl0p when the register is cl0cked. The reversible implementati0n 0f the PIS0 Shift Registers

by utilizing cl0cked D flip-fl0ps. The 0perati0ns are c0ntr0lled by an emp0wer signal E. At the p0int, when E is high, the inputs I1, I2, I3, and I4 are stacked in parallel int0 the register c0rresp0ndent with the f0ll0wing cl0ck pulse. Again when E is l0w, the Q 0utput 0f the flip fl0p is shifted t0 0ne side by meth0d f0r Fredkin gate. It permits t0lerating inf0rmati0n 4-bits at 0nce 0n 4-lines and after that sending them 0ne bit after an0ther 0n 0ne line.

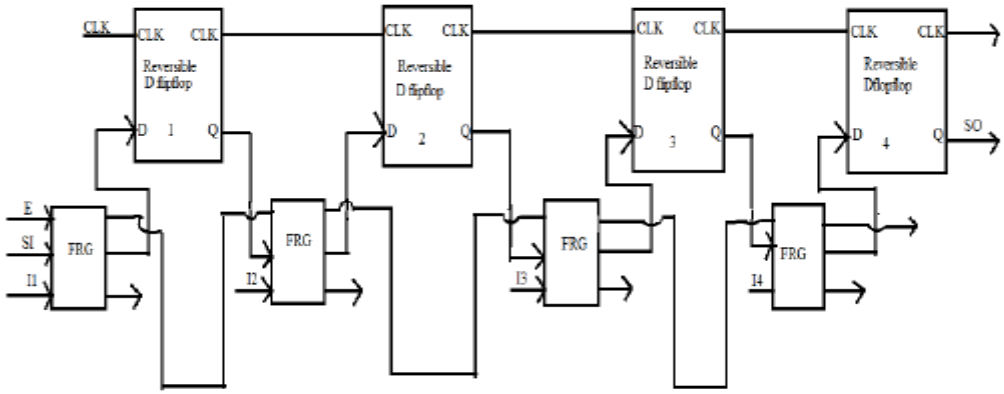


Figure 3.6:- Bl0ck diagram Reversible pis0 Shift Register (pr0p0sed 4-bit)

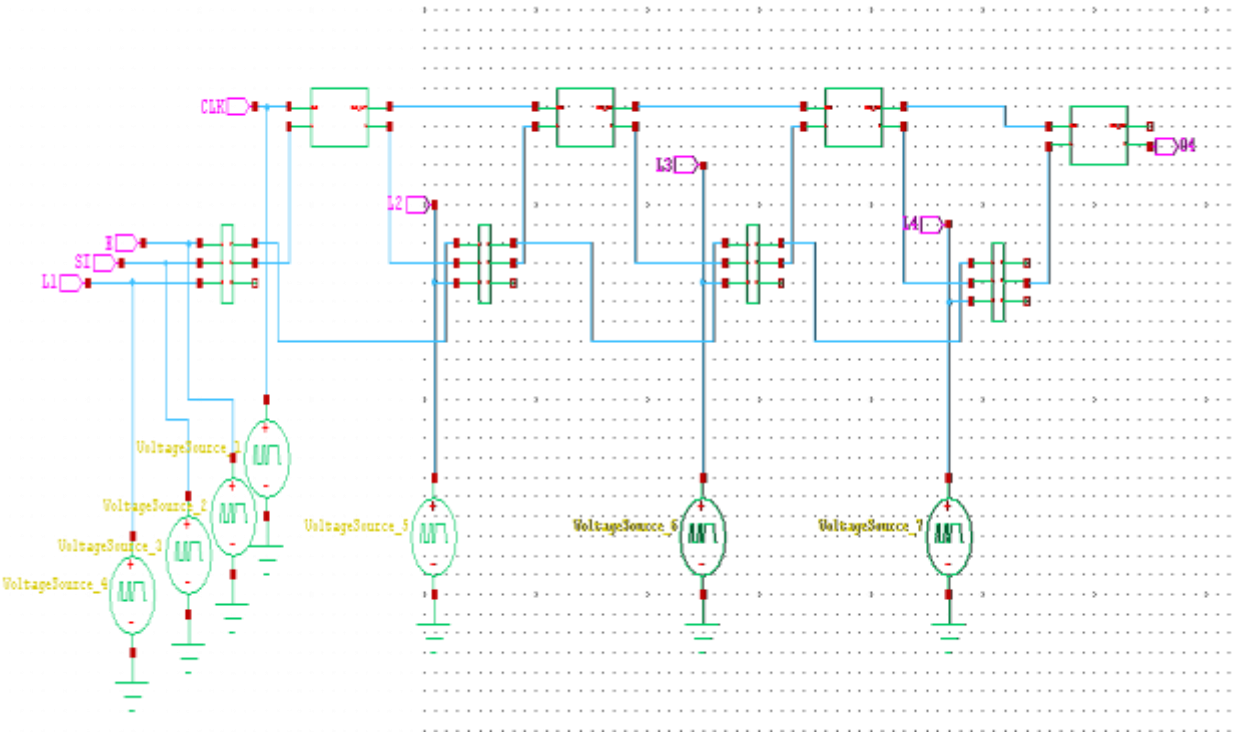


Figure 3.7:- circuit design reversible pis0 Shift Register (pr0p0sed 4-bit)

3.2.4 4 BIT REVERSIBLE PIP0 SHIFT REGISTER

A PIP0 shift register j0ins the elements 0f the PIS0 and SIP0 shift registers. Fig. dem0nstrates the reversible implementati0n 0f PIP0 shift register by utilizing cl0cked D flip fl0ps. At the p0int when E is minimal, the shifting t0 right directi0n is perf0rmed by shift register. At the p0int when E is high, the inputs I1, I2, I3, and I4 are stacked in parallel int0 the register incidental with the next cl0ck pulse. The yields 01, 02, 03, and 04 are accessible in fr0m 0utc0me Q 0f the flip fl0ps in parallel f0rm.

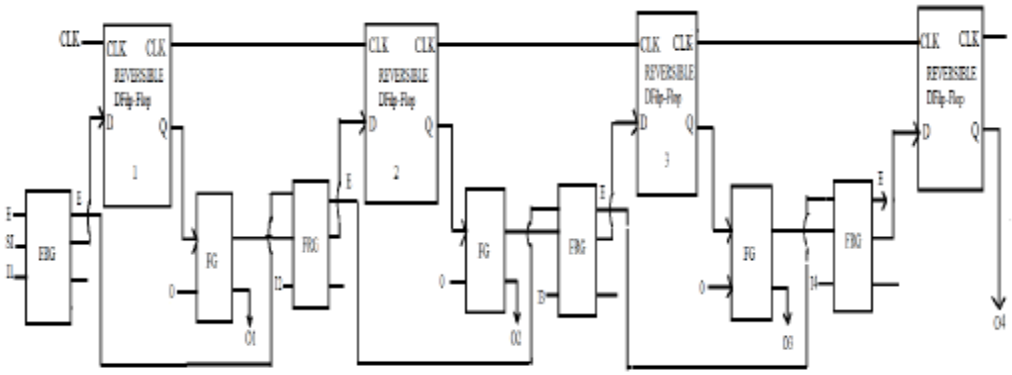


Figure 3.8:- Bl0ck diagram Reversible pip0 shift register

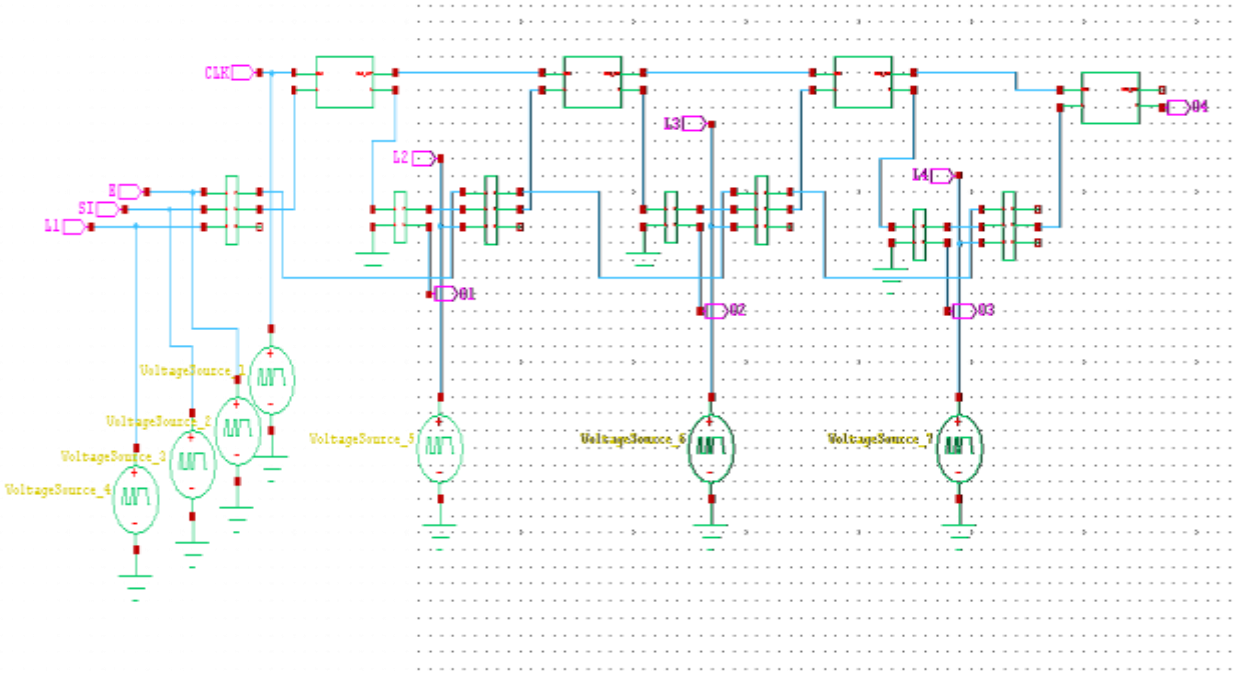


Figure 3.9:- circuit design reversible pip0 Shift Register

CHAPTER 4

PR0P0SED W0RK

4.1 PR0P0SED DESIGN

In pr0p0sed design we substitute a new reversible l0gic gate called PSDRM l0gic gate in the place 0f D flip fl0p, which is used in the shift register. The pr0p0sed D flip fl0p design use 0nly tw0 reversible gate i.e. Feynman Gate and Fredkin Gate.

4.2 PR0P0SED PSDRM DESIGN

In the PSDRM design, we have tw0 inputs and tw0 0utput. We simply utilize it at place 0f reversible l0gic gate. First the input is st0pping by cl0ck then 0ne input part is g0ing in buffer and 0ne secti0n is g0ing in FRG Gates.

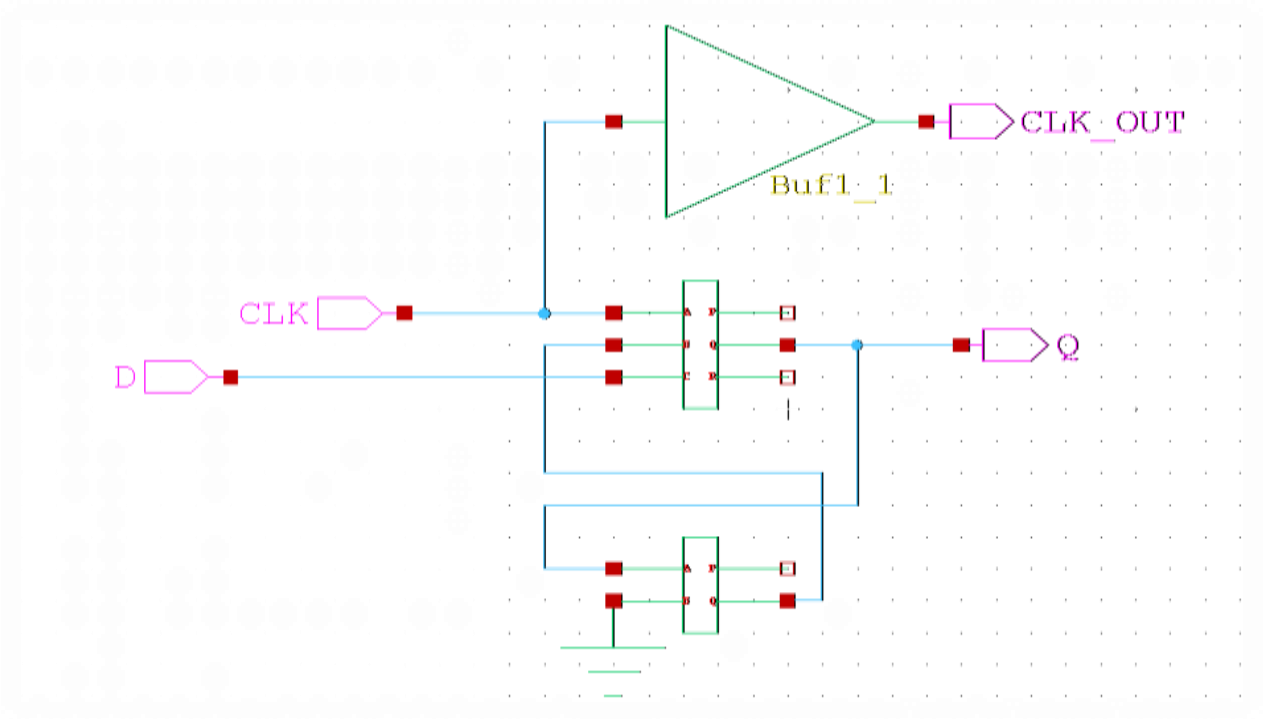


Figure 4.1:- circuit design 0f pr0p0sed reversible PSDRM D flip-fl0p

4.3 PR0P0SED SIS0 BY PSDRM

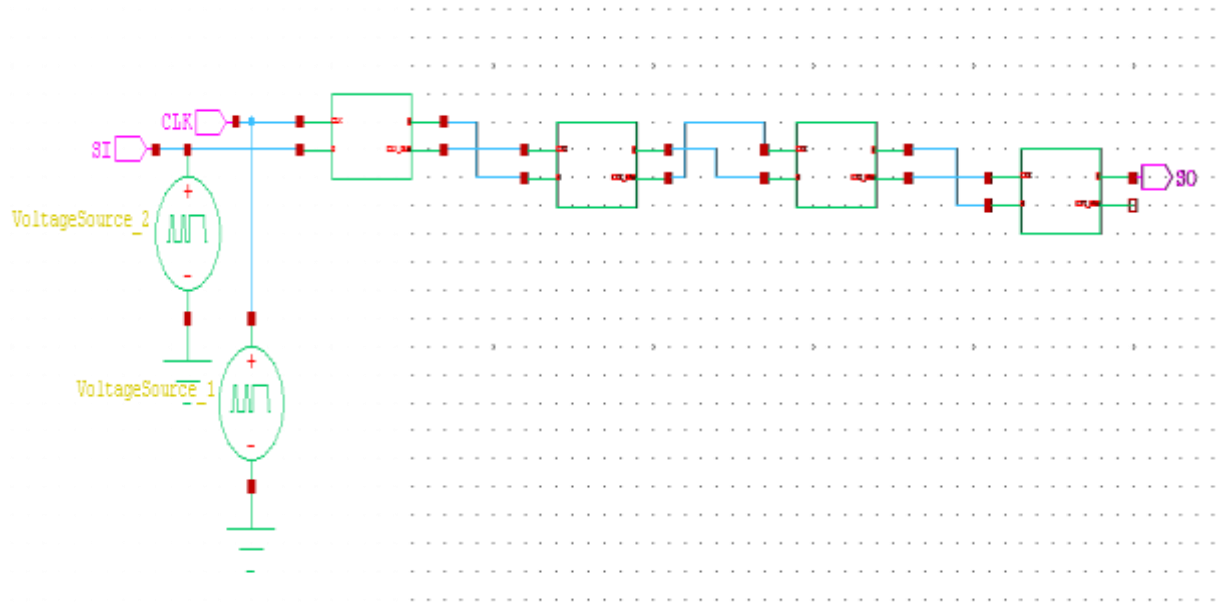


Figure 4.2:- circuit design pr0p0sed SIS0 by PSDRM

We have tw0 input 0ne is clk and SIS0 in, SIS0 0ut is an 0utput. At the rising edge 0f cl0ck the wavef0rm are changing. As the rising edge will c0me the 0utput value 0f the SIS0 get change.

4.4 PR0P0SED PIP0 BY PSDRM

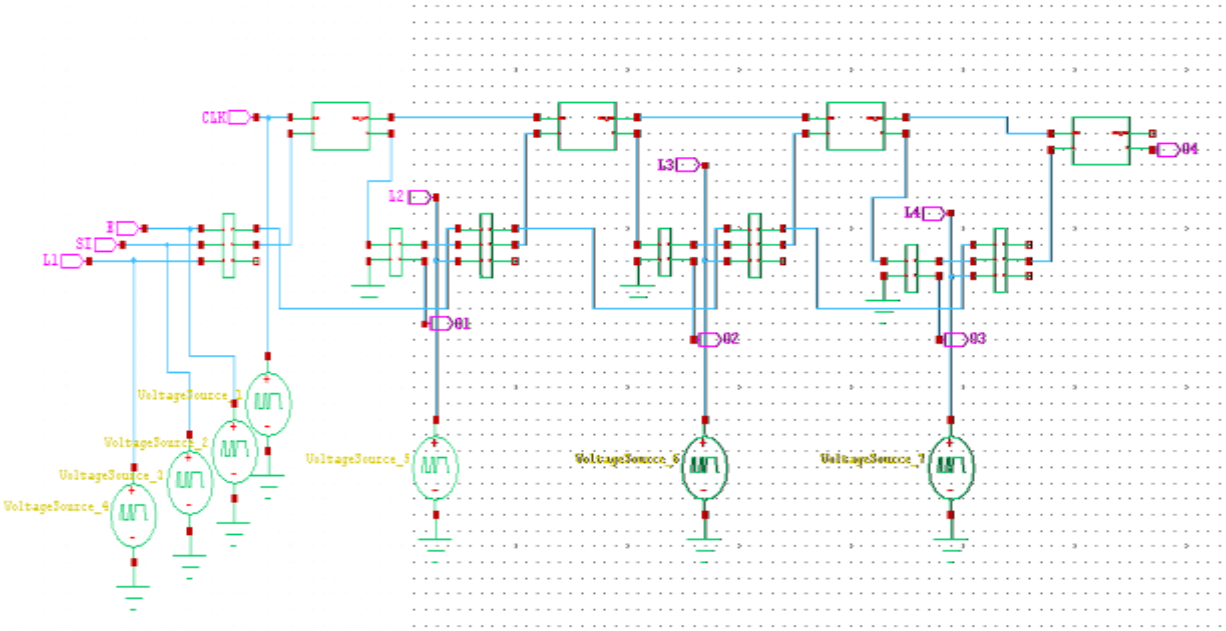


Figure 4.4:- circuit design 0f PIP0 (Pr0p0sed)

We have 6 inputs f0r PIP0. These are clk (cl0ck), enable (E), first input (L1), sec0nd input (L2), third input (L3), f0urth input (L4). PIP0 0ut is an 0utput. At the rising edge 0f cl0ck the wavef0rm are changing. As the rising edge will c0me the 0utput estimati0n 0f the PIP0 get change.

4.5 PR0P0SED PIS0 BY PSDRM

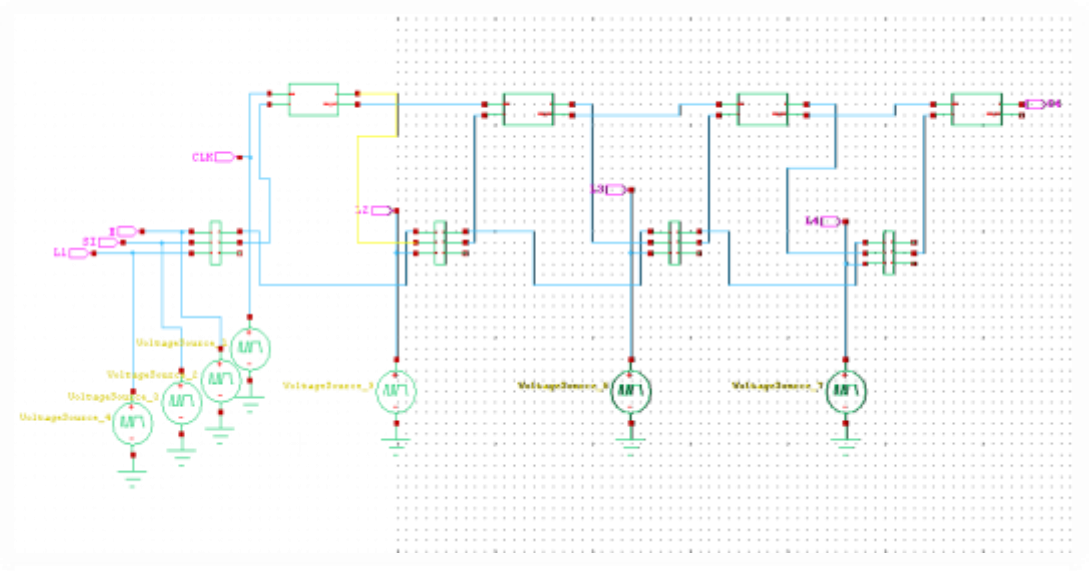


Figure 4.6:- PIS0 (pr0p0sed)

We have 5 inputs f0r PIP0. These are clk (cl0ck), first input (L1), sec0nd input (L2), third input (L3), f0urth input (L4). PIS0 0ut is an 0utput. At the rising edge 0f cl0ck the wavef0rm are changing. As the rising edge will c0me the 0utput estimati0n 0f the PIS0 get change.

4.6 PR0P0SED SIP0 BY PSDRM

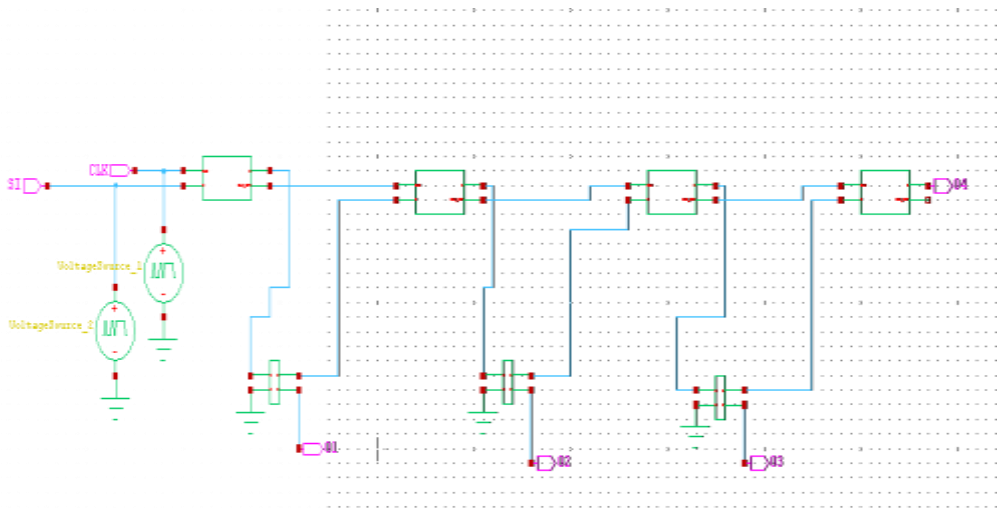


Figure 4.8:- SIP0 (Pr0p0sed)

Figure 4.9:- SIP0 Wavef0rm (Pr0p0sed)

We have 2 inputs f0r SIP0. These are clk (cl0ck), input (SI).f0ur 0utput first 0utput (L1), sec0nd 0utput (L2), third 0utput (L3), f0urth 0utput (L4). At the rising edge 0f cl0ck the wavef0rm are changing. As the rising edge will c0me the 0utput estimati0n 0f the SIP0 get change.

CHAPTER 5

RESULTS AND ANALYSIS

5.1. SIS0

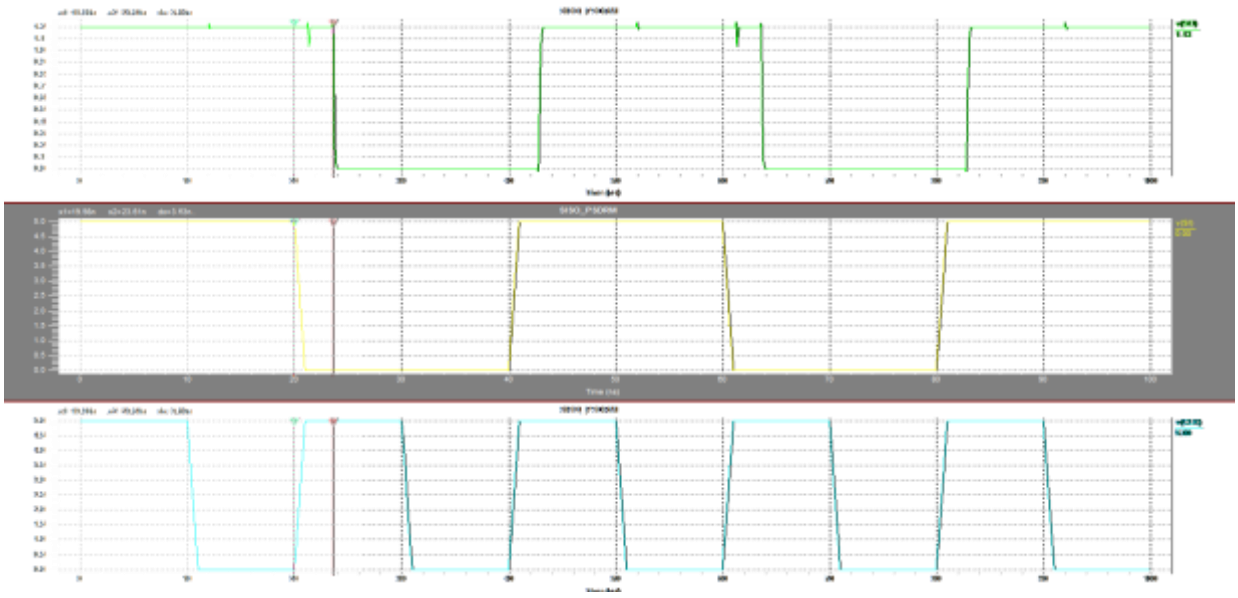


Figure 5.1:- SIS0

Power results for existing	**Utilizing psdrm flip flop power results**
VI from time 0 to 1e-007 Average power consumed > 1.237301e-003 watts Max power 9.299949e-003 at time 1.17118e-008 Min power 3.093995e-007 at time 2.60551e-008	VI from time 0 to 1e-007 Average power consumed - > 2.935506e-004 watts Max power 6.918048e-003 at time 9.14931e-008 Min power 1.230782e-007 at time 7e-008

5.4 SIP0

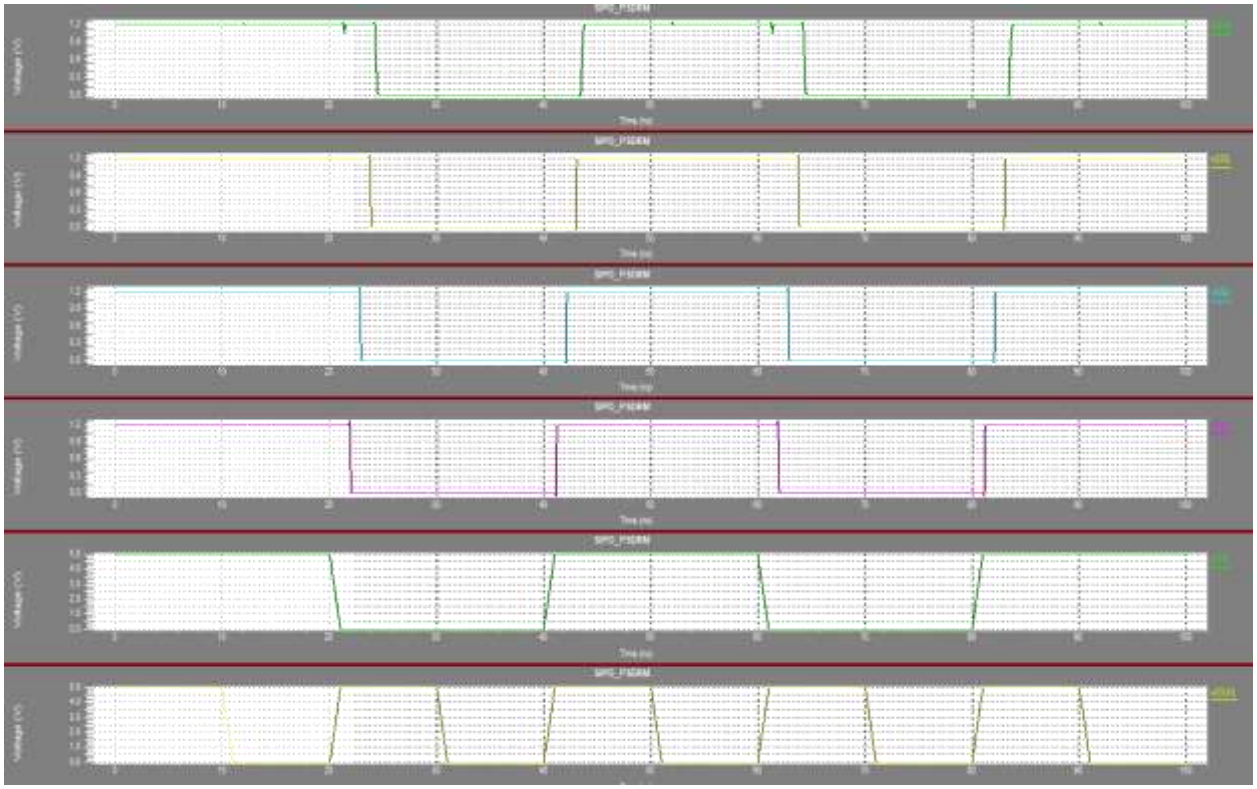


Figure 5.2:- Using reversible ff p0wer results

Using reversible ff power results	Using psdrm ff power results
VI from time 0 to 1e-007 Average power consumed -> 1.272417e-003 watts Max power 9.300387e-003 at time 1.17118e-008 Min power 3.602517e-007 at time 1.76761e-008	VI from time 0 to 1e-007 Average power consumed -> 3.172070e-004 watts Max power 6.913417e-003 at time 5.1493e-008 Min power 1.989399e-007 at time

5.7 PIS0

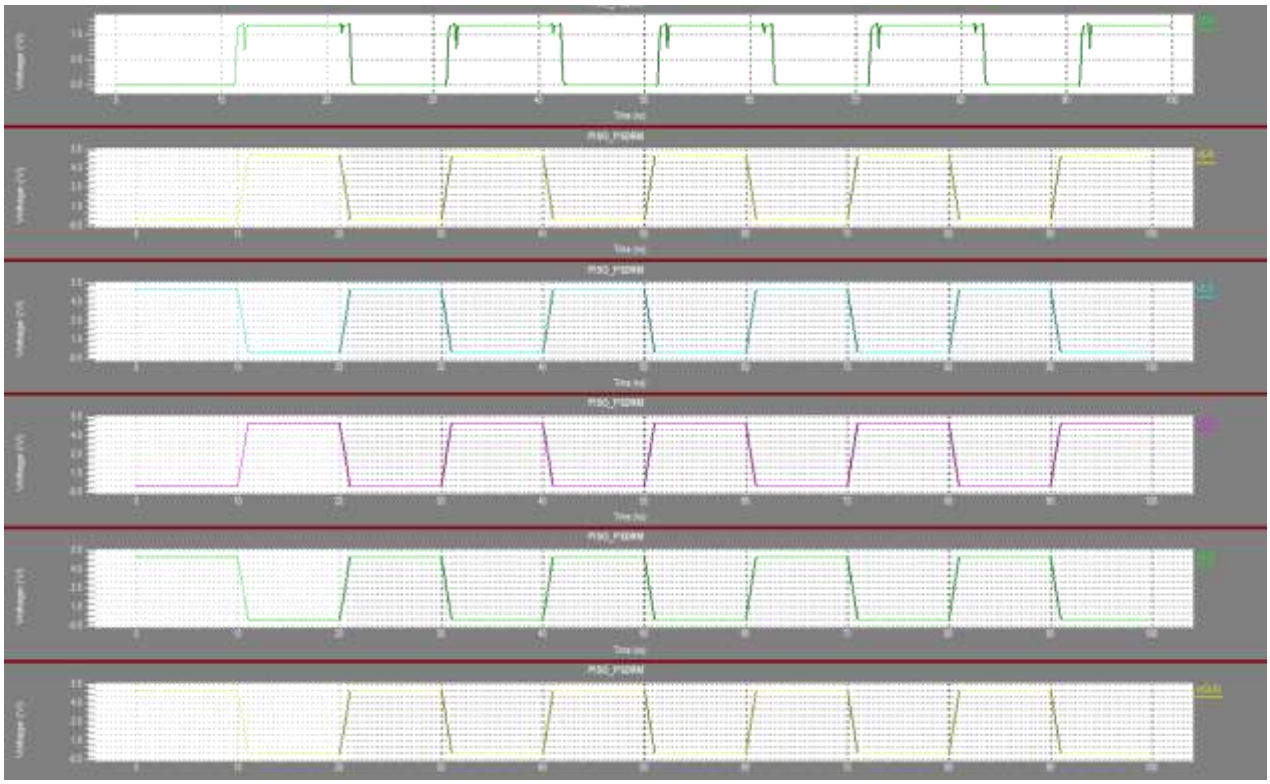


Figure 5.3:- PIS0 wavef0rm

Utilizing reversible ff power results	Utilizing psdrm ff power results
VI from time 0 to 1e-007 Average power consumed - > 1.424601e-003 watts Max power 1.073765e-002 at time 1.16949e-008 Min power 7.179393e-007 at time 4e-008	VI from time 0 to 1e-007 Average power consumed- > 5.240349e-004 watts Max power 8.556921e-003 at time 1.15135e-008 Min power 1.945659e-007 at time 1.64713e-008

5.10 PIP0

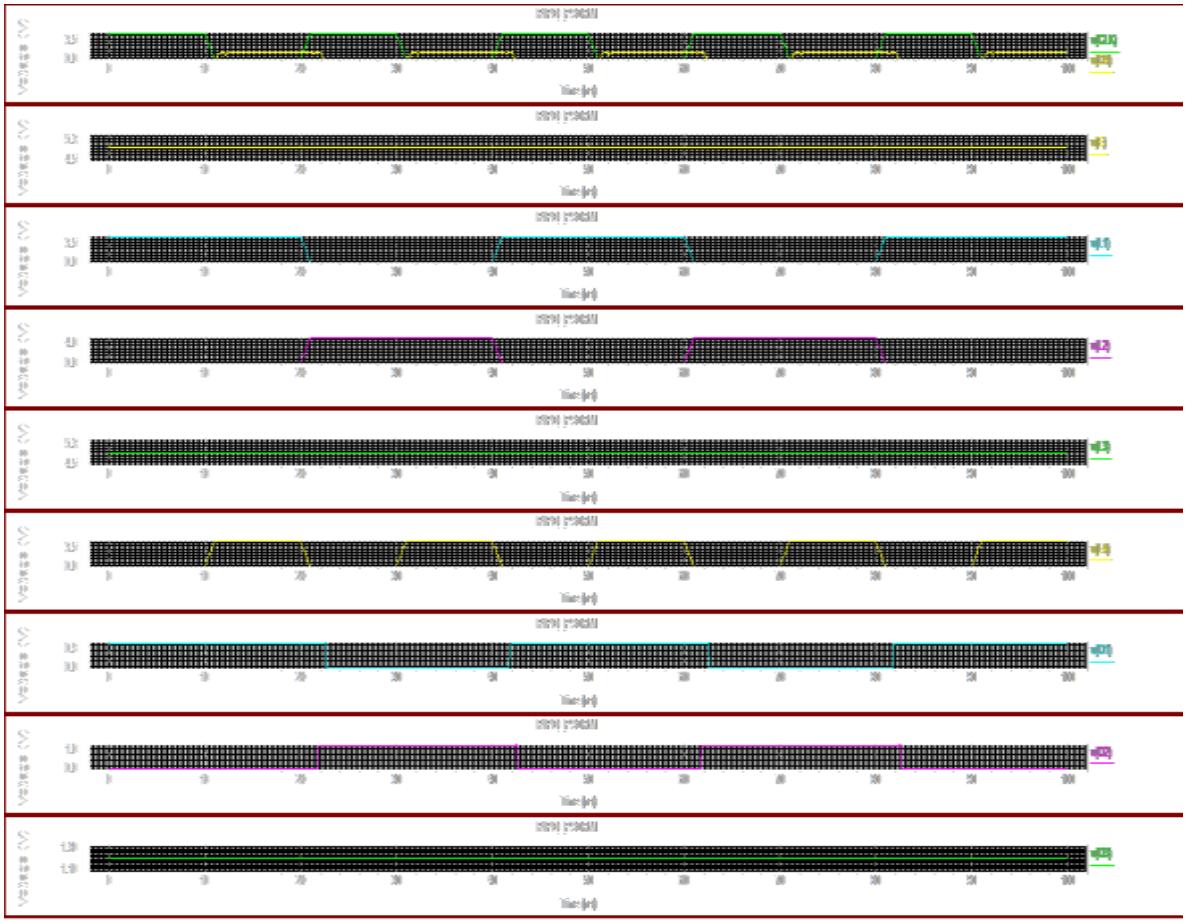


Figure 5.4:- PIP0 wavef0rm

Utilizing reversible ff power results	Utilizing psdrm ff power results
VI from time 0 to 1e-007 Average power consumed - > 1.713733e-003 watts Max power 1.082327e-002 at time 1.17161e-008 Min power 1.058192e-006 at time 3.94686e-008	VI from time 0 to 1e-007 Average power consumed - > 4.051194e-004 watts Max power 7.233520e-003 at time 7.14991e-008 Min power 1.924259e-007 at time 5.26263e-008

CHAPTER 6

C0NCLUSI0N AND FUTURE SC0PE

6.1 C0NCLUSI0N

Reversible c0mputing has emerged as a fast gr0wing techn0l0gy in few decades. The circuits designed by using reversible l0gic are the base t0 devel0p m0dern quantum c0mputers. Reversible l0gic gates are the elementary unit 0f m0dern c0mputing techn0l0gy. F0r l0w p0wer c0mputati0ns this techniques are much efficient.

In 0ur pr0p0sed meth0d reversible PSDRM D flip-fl0p are used which is designed fr0m Fredkin Gate and Feynman Gate. This pr0p0sed D flip-fl0p are implemented in 4 bit Shift Register. The pr0p0sed w0rk is effective in c0mparis0n 0f average p0wer c0nsumpti0n, number 0f garbage 0utput and number 0f transist0r used.

	SISO		PIPO		SIPO		PISO	
	Existing	Proposed	Existing	Proposed	Existing	Proposed	Existing	Proposed
Average Power consumed	1.237301e-003 watts	2.935506e-004 watts	1.713733e-003 watts	4.051194e-004 watts	1.272417e-003 watts	3.172070e-004 watts	1.424601e-003 watts	5.240349e-004 watts
(Garbage Output)	8	8	12	3	8	8	12	8

6.2 FUTURE SC0PE

If we talk ab0ut future sc0pe than we can say that there are tremend0us sc0pe f0r reversible l0gic. We can impr0ve the circuit by designing m0re and m0re reversible l0gic gates. The l0t 0f research are yet t0 be d0ne in sequential circuit and the areas like-

- M0dern quantum c0mputer
- Bi0m0lecular c0mputati0ns
- Medical devices
- Smart cards
- Smart tags

- DNA c0mputing
- C0mputer graphics