ABSTARCT

A Flip Flop on the dual edge & minimal power constituted on feed of signal is suggested. Absorption of power is the main concern in design of a circuitry. The design as suggested minimizes power in contrast to FFs triggered on explicit pulses. Greater speed of operation can be attained by raising the quantity of path of charging & transistors in contrast to other FFs. Flip flops as DETFFs are taken as to save power. Designs that are on dual edges work out on a range of lessen voltage & so are taken as a good match for applications with lessens voltages. These FFs make use of transistors with a delicate feedback & having to stable absorption of power. This brings down current of leakage & so save the power. By making use of clocks with minimal frequency, greater efficiency can be attained. Tools of tanner 14 are employed with technology of 45nm CMOS to implement simulations. In this document, a new methodology for implementation of lessen energy FFs on dual edges is observed. Also a new schema for sharing of branch on clocks is employed for deduction n quantity of transistors that are clocked in design. The design as suggested also deploys a discharge on conditions & terminologies on splitting of paths that will deduce switching & currents on short circuits.

Keyword :-—CMOS, double edge, flip-flop, low power.

CHAPTER 1

INTRODUCTION

FFs are generally taken as implementation of logics gates. A memory can be formulated by implementing logics of Boolean. They can also be taken as the base of RAM. All the values that are furnished to them in form of inputs will be retained & implemented is the structure of gates on logics is exact. An enhanced version of applications on FFs will help out for improvisations in designs.

The main implementation of FFs is in the circuitries to provide feedback. The basic concept of memory is feedback, so FFs can be designed & implemented to it.

There are 4 main FFs that are employed in circuitries which are said as:

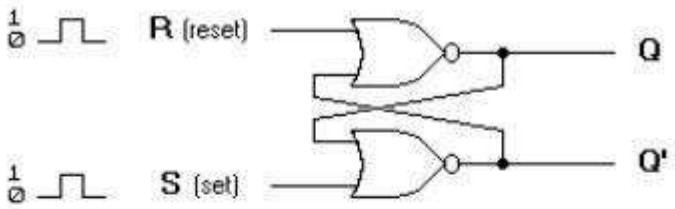
1. A standard S-R FF.
2. D-FF.
3. J-K FF.
4. T-FF.

1.1 S-R FLIP FLOP

The S-R or set reset FF is formulated by taking gates of NOR & NAND two in number. This FF is also termed as latch of S-R FF.

1.1.1 S-R FLIP FLOP USING NOR GATE

There are two inputs in structure of this FF which are termed as reset & set. Also two outcomes denoted as Q' & Q. Truth table & diagram are as presented.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	

(b) Truth table

Basic flip-flop circuit with NOR gates

Fig 1.1 :- S-R Flip Flop using NOR Gate

The FF has four stages as revealed by the diagram described as:

S=1, R=0---Q, Q'=0

This is also termed as state of 'set'.

S=0, R=1---Q=0, Q'=1

This is also termed as state of 'reset'.

In all states, it is observed that outcomes are complementary to the one another & values of Q gets along that of S.

S=0, R=0---Q, Q'= Remember

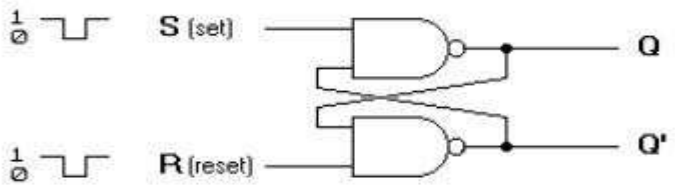
As switching of values of R & S is made 0, and then earlier states are considered by circuitry.

S=1, R=1---Q, Q'=0 which is invalid.

This state is invalid as Q & Q' both have value as 0 where there values should be complimentary to one another. This state has to be eliminated.

1.1.2 S-R FLIP FLOP USING NAND GATE

The S-R FF circuitry by NAND gate is presented below:



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	

(b) Truth table

Basic flip-flop circuit with NAND gates

Fig 1.2 :- S-R Flip Flop using NAND Gate

Similarly to NOR gated FF, there are 4 states in this as well.

S=1, R=0---Q, Q'=1

This is also termed as state of 'set'.

S=0, R=1---Q=0=1, Q'=0

This is also termed as state of 'reset'.

In all states, it is observed that outcomes are complementary to the one another & values of Q gets along that of S.

S=0, R=0---Q, Q'=1 which is invalid.

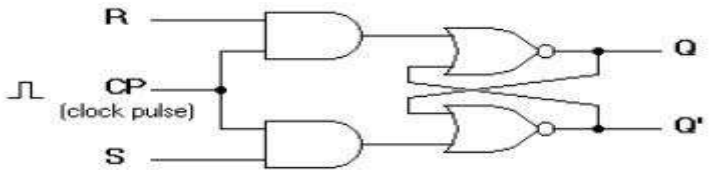
If both the values of S and R are switched to 0 it is an invalid state because the values of both Q and Q' are 1. They are supposed to be compliments of each other. Normally, this state must be avoided.

S=1, R=1—Q & Q'= Remember

This state is invalid as Q & Q' both have value as 1, circuitry will opt the earlier state of R & S.

1.1.3 CLOCKED S-R FLIP FLOP

It is also termed as S-R FF that is gated. The issue that FF of S-R faces is when there is a state which is not valid. This issue can be solved by employing a FF of S-R with bilateral stability that can transform outcomes even when states that are not valid are incurred even without considering inputs of reset & set. For this purpose a FF which is clocked is formulated by summing up two gates of logic of AND to a standard gate of NOR. The diagram of circuitry & table are as presented.



(a) Logic diagram

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

(b) Truth table

Clocked SR flip-flop

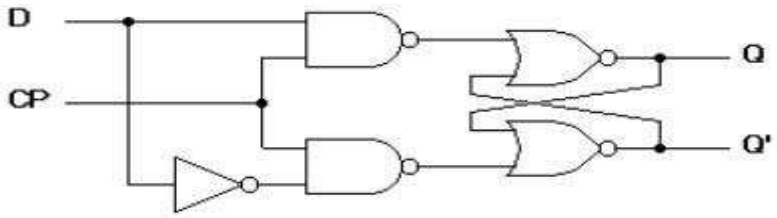
Fig 1.3 :- Clocked S-R Flip Flop

A pulse of clock is furnished to AND logical gate. As the value accumulated by pulse of clock gets 0, outcomes of gates of AND will be set as 0. The CP will turn out to be 1 as pulse is

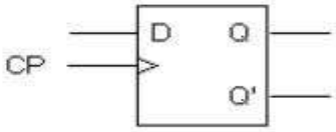
provided to it. This forms R & S values to go & cross through gates of NOR FF. as the R &S values become 1, the value of CP that is high become 0 for some time. As pulse gets eliminated, state of FF will turn to be neutral. So one of the two states will incur & it relies on that if state of reset or set in FF goes as 1 that is even greater than 0 transitions at extinction of pulse. So the states which are not valid can be get rid off.

1.2. D FLIP FLOP

Design of circuitry & truth table for this FF is presented below:



(a) Logic diagram with NAND gates



(b) Graphical symbol

Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Transition table

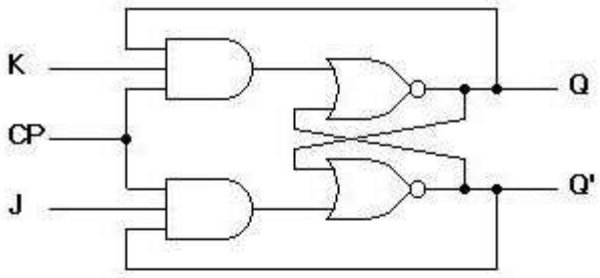
Clocked D flip-flop

Fig 1.4 :- D Flip Flop

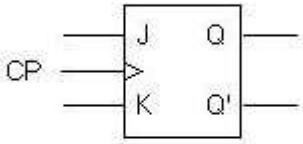
FF of D is formulated by making generally small transformations in FF of R-S. By the diagram it is evident that input D is linked to S & its complimentary is linked to input R. the input of D is forwarded to FF as CP goes to 1. As state of CP gets high, FF is in state of set. If the value of CP is 0, FF has the state as clear.

1.3. J-K FLIP FLOP

The diagram of circuitry & truth table of FF of J-K is presented as:



(a) Logic diagram



(b) Graphical symbol

Q J K	Q(t+1)
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	0
1 1 0	1
1 1 1	0

(c) Transition table

Clocked JK flip-flop

Fig 1.5 :- J-K Flip Flop

A FF of J-K can be termed as transformation to FF of R-S. The only & basic difference they have is state of intermediation is finer & accurate than S-R FF.

Working of J & K is similar to that of inputs of R & S. In this FF, J denotes set & K denotes clear.

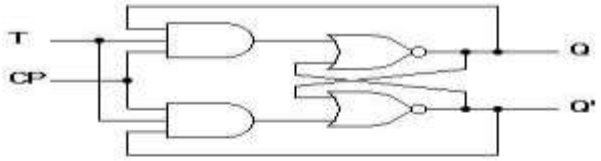
As both inputs of K & J is high, state of FF will be turned as complement. As when Q is 1, it will be turned to 0 & vice versa.

The circuitry is comprised of 2 gates of AND with 3 inputs. The outcome of Q by FF is turned to as feedback of input to AND by the inputs similar to K & CP. Thus, as CP goes to 1, state of FF will become clear with a constraint that Q must be 1 before that. Parallel to this, outcome of FF as Q' must be furnished to input as feedback of AND by various inputs like CP & J. Thus as CP becomes 1, outcome will be set & only when if Q'1 was 1 before that.

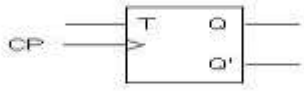
This outcome can get repeated when their complement has been taken as J=K=1 as by the link of feedback in FF of J-K. This situation can be eliminated by taking duration of time less than the delay in propagation through FF. Constraints on the width of pulse can be get off by formulating a FF of master & slave or triggered on edge.

1.4. T FLIP FLOP

This is the simplest version of FF of J & K. Both inputs of J & K will be interlinked & so it is also termed as a J & K FF with a single input. As pulse of clock is furnished to FF, toggling in outcomes started. Thus the constraints on width of pulse can be abolished with formation of edge trigger or master & slave. Presentation of truth table & circuitry is as:



(a) Logic diagram



(b) Graphical symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

(c) Transition table

Clocked T flip-flop

Fig 1.6 :- T Flip Flop

1.5 EDGE-TRIGGERED DYNAMIC D STORAGE ELEMENT

The best alternate provided to a FF of type D can be formulated by the circuitries which are dynamic as long their clocking is done while its not a FF in actual but still termed as that because of its functionality. As the element of D on master & slave gets triggered on clock edge, the constituents are triggered on levels of clock. This FF though is not a real FF doesn't possess characteristics of master & slave.

The FFs of type D which are triggered on edge are executed on operations that require greater speed by making use of logics that are dynamic. It reveals that outcome of digital format is accumulated on capacitance of devices which are parasitic type & since no transition is taking place by the device. Structure of FFs which are dynamic initiates resetting in a simple mode as the operation for resetting can be executed by discharging many nodes linked internally.

A basic type of FF that is dynamic is of type TSPC that executes operations of FFs with minimal power & greater speed. Though FFs which are dynamic don't operate at constant or lessen speed of clocks when provided complete time, paths of leakages can discharge capacitance which is much enough for FF to go to state of invalid.

The FF that is of type triggered makes changes to states on either edge of positive or negative type on pulse of clock on input of control. The standard forms are presented here: D, S-R & J-K.

The inputs of these inputs are termed as synchronous as information accumulated on these inputs is shifted to outcome of FFs only on the edge that triggers on pulse of clock. While input of SET & CLR is termed as asynchronous as they put an impact on FF's state & are not dependent on clock. The inputs which are asynchronous should be kept minimum so applications that are synchronous can work fine.

1.6 EDGE-TRIGGERED S-R FLIP-FLOP

Standard functioning is explained along the truth table for this FF. truth table & operation of both positive & negative edge FF is similar except that the edge falling in pulse of clock is edge that triggers.

Inputs			Outputs		
S	R	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

Table 1.1 :- EDGE-TRIGGERED S-R FLIP-FLOP

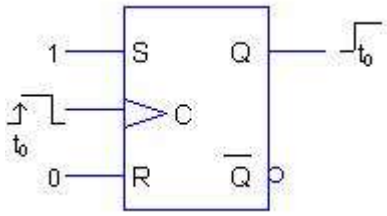


Fig 1.7 :- S-R FLIP-FLOP

If S=1 & R=0, FF is set on rising edge of clock.

It is to be noted that inputs of R & S can fluctuate at any instance when input of clock is either high or low with no impact on outcome. The diagram of timing is presented as:

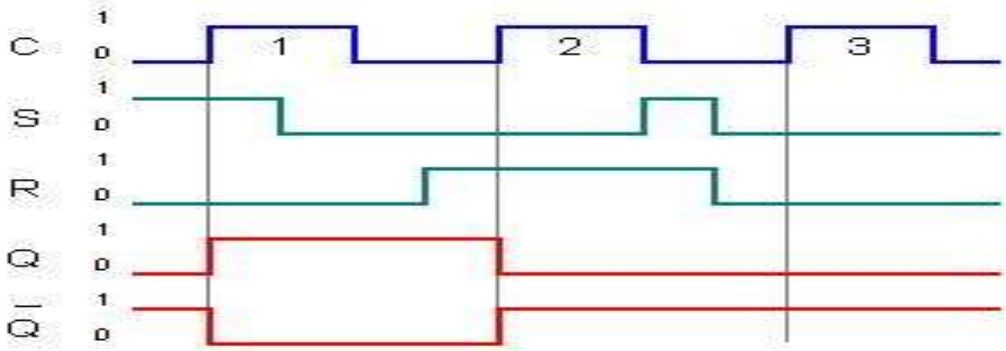


Fig 1.8 :- S-R based flip flop

1.7 EDGE-TRIGGERED J-K FLIP-FLOP

The working of FFs of S-R & J-K is same. Key difference in both is that there is no state that is invalid. As both inputs of J & K will be high, outcome will toggle. Its truth table is as:

Inputs			Outputs		
J	K	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q'	Q	Toggle

Table 1.2 :- Edge triggered J-K Flip Flop

1.8 EDGE-TRIGGERED D FLIP-FLOP

Working of FF D is very simple. There is one more input to clock. And its usage for retaining bits of data is immense. As is the input of D is high on implementation of pulse of clock, state of FF is set & it accumulates 1. If state of input D is low on implementation of pulse of clock, state of FF is reset & it accumulates 0. The summary of truth table on functioning of FF of type D on edge that is positive. Before that, functioning of FF on edge of negative type is same but difference is that in this, pulse of clock is triggered on the edge that is falling.

CHAPTER 2

LITERATURE REVIEW

[2.1] 2014 " Design of Low Power Dual Edge Triggered Flip Flop Based On Signal Feed through Scheme " S.Sujatha , International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 11, November 2014:- A Flip Flop on the dual edge & minimal power constituted on feed of signal is suggested. Absorption of power is the main concern in design of a circuitry. The design as suggested minimizes power in contrast to FFs triggered on explicit pulses. Greater speed of operation can be attained by raising the quantity of path of charging & transistors in contrast to other FFs. Flip flops as Dual Edge Triggered Flip Flops abbreviated as DETFFs are taken as to save power. Designs that are on dual edges work out on a range of lessen voltage & so are taken as a good match for applications with lessens voltages. These FFs make use of transistors with a delicate feedback & having to stable absorption of power. This brings down current of leakage & so save the power. By making use of clocks with minimal frequency, greater efficiency can be attained. Tanner EDA Tool v14 are employed with technology of 90nm CMOS to implement simulations.

The absorption of power dynamically in tree of clock relies upon the frequency & load on a clock tree. If on both rising & falling edge, sampling is performed for input [3], this clock would be having half of the frequency of the clock that is triggered on a single edge FF that is also termed as Double edge triggered FF. Double edge triggered FF abbreviated as DETFF absorbs minimal dynamic power, delay & static power in contrast to the FFs that were designed previously. DETFF are gaining popularity for the designs that has less power as the frequency of clock is required to be halved. Two latches that are transparent are put in parallel to each other to design a DETFF where as for a single edge FF, the latches are placed in series. DETFF pass on the information to both of the edges that are negative & positive. This provides assistance to several applications where efficacy needed is much greater. FFs are considered as cardinal elements to store data in digital format circuitries that are employed for speed & absorption of power. An alternate approach for clocking makes use of DETFF that accumulates the information on both falling & rising edges of clock. Similar efficient information can be attained at half of the clock frequency in contrast to single edge triggered FF. it can be said that clocking

on double edge can be employed to save around 50% of the power & supplied voltage is a factor that determines leakage of power.

2.1.1 CONVENTIONAL EXPLICIT TYPE P-FF DESIGNS

Figure 2.1 presents a traditional approach of explicit type that is closely related to outcome. It is comprised of pulse generator that is constituted on NAND logics & a semi dynamic true single phase clock abbreviated as TSPC. In this design of PFF, inverters of I3 & I4 are deployed to accumulate information while inverters I1 & I2 accumulate the X that is internal node. The width of pulse is computed by delay of the 3 inverters. Even it has got a drawback if static input is 1 & the node of X gets dispense on every rising edge if clock. There are few methodologies that are employed to cope up with this problem. They are conditional on discharge, precharge & capture & schema for enhancement of pulse. [2].

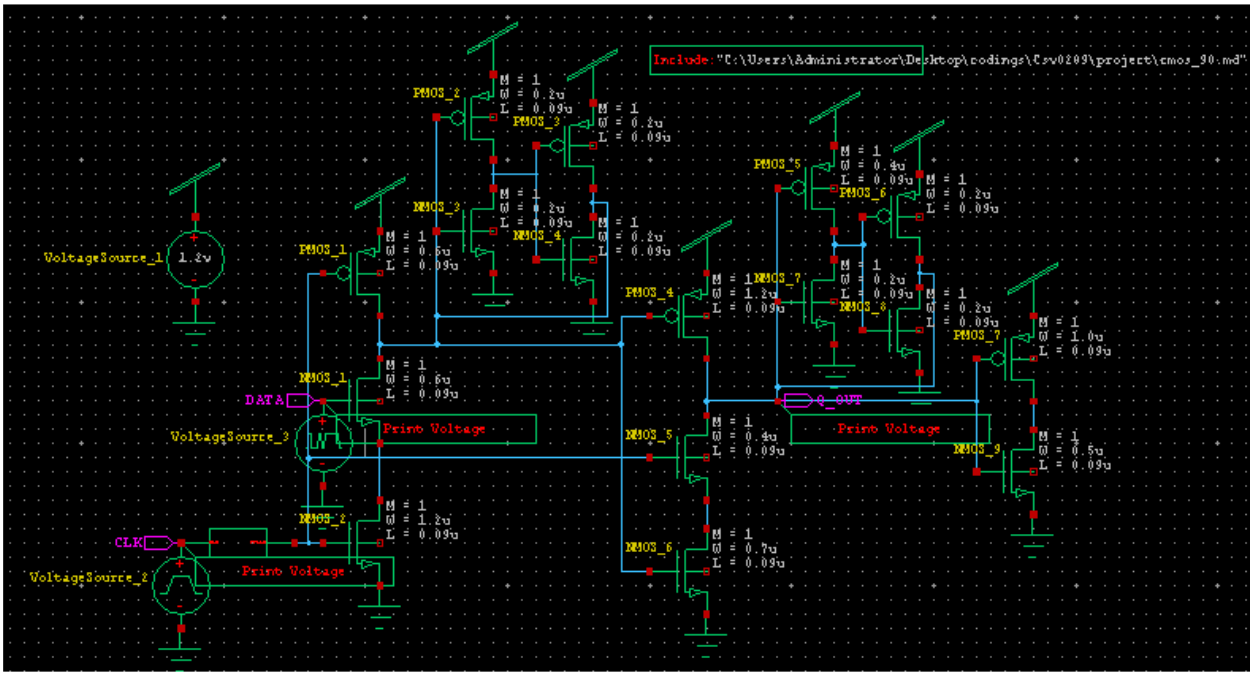


Fig.2.1. ep-DCO

Figure 2.2 presents the methodologies of conditional discharge. It retains more information to delay of Q in contrast to CDFF. As there are stacked transistors, 3 in number are employed that face the worst delays. To cope up with this delay issue, a circuitry of pull-down is employed but there are few disadvantages that has some relation to absorption of power & additional area of layout.

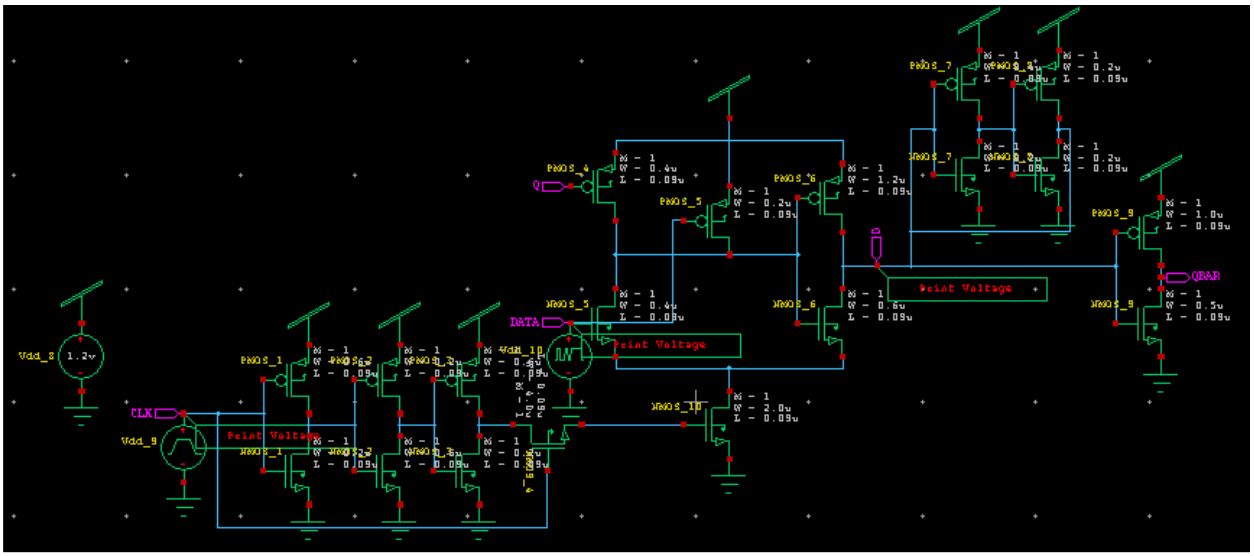


Fig.2.2 : Static-CDFF

The MHLFF that is modified hybrid latch-FF as presented in Figure 3. There is elimination of keeper logic at node X. It is even satisfied by a weak pull up transistor that is MP1 which is regulated by the outcome signal. So Q sustains the node X level when Q is equal to 0. The design of MHLFF has got 2 drawbacks. Before that, prolonged delay of 0 to 1 is presumed. The second node X tends to be floating on some instances & value of it can be varied by some additional power of dc current.

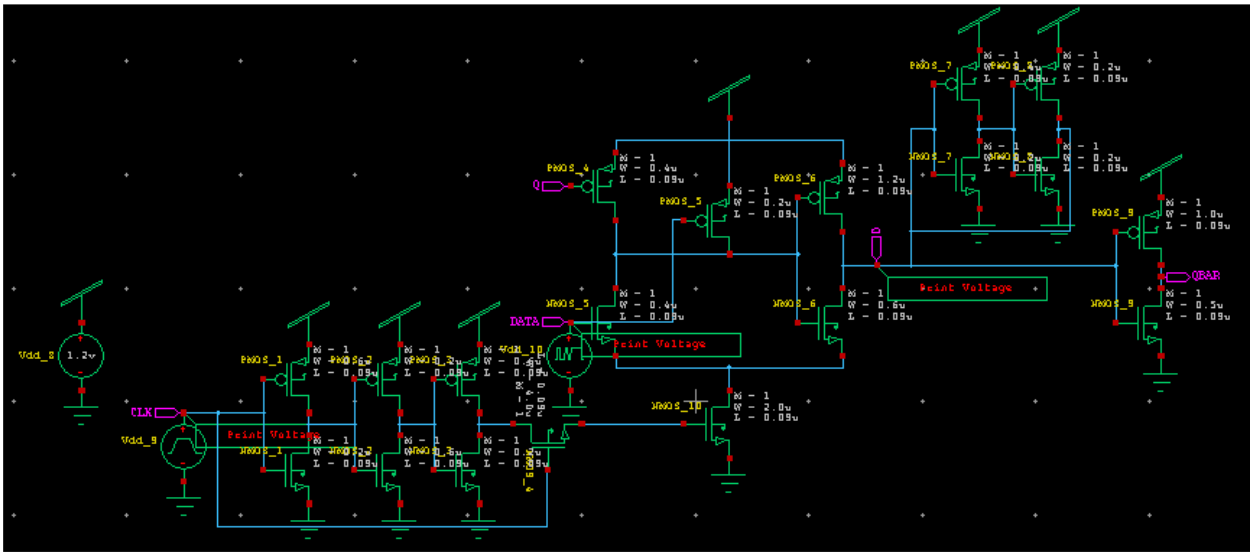


Fig.2.3:- . MHLFF

2.1.2 PULSE TRIGGERED FLIPFLOP

The pulse triggered FF having a signal feed is employed for deduction of delay when transition is faced up in data through a schema [1]. The signal feed by a schema is comprised of pass transistors as presented in Figure 4. It visualize the pulse triggered FF.

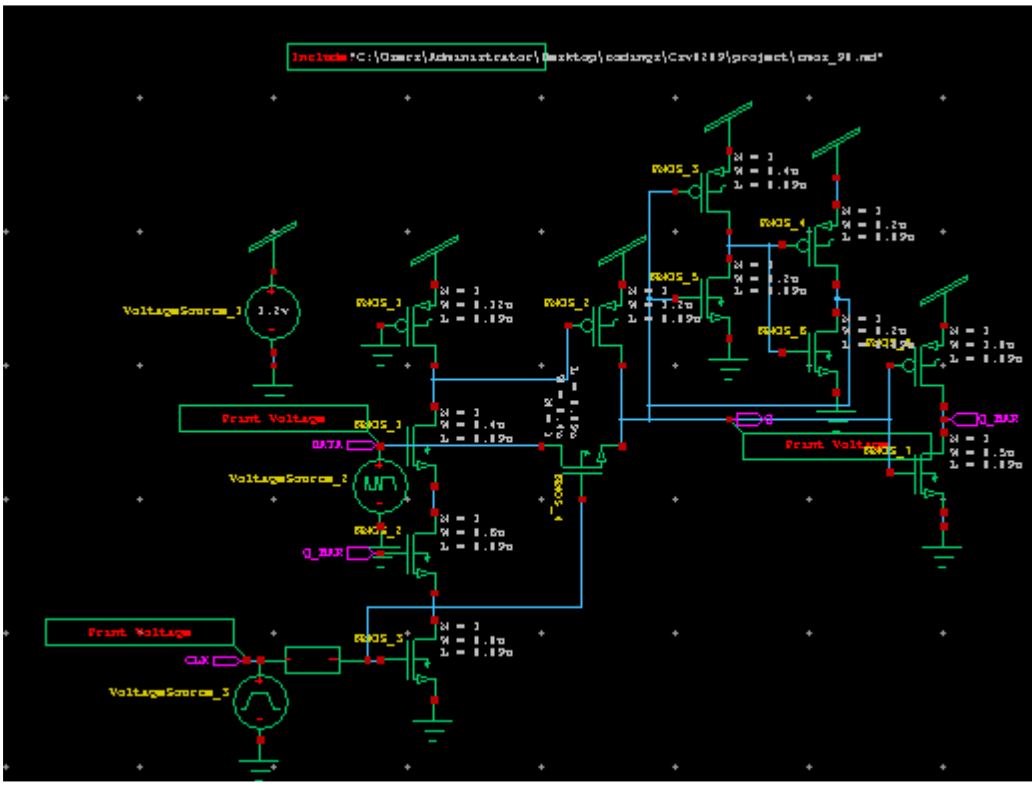


Fig.2.4. pulse triggered FF

This design has got some main contrast in contrast to other circuitries.

- At first the PMOS transistor on weak pull up is prevented. In this, an imitated logic style of NMOS escorted & so node X that is internal is retained.
- Secondly a pass transistor is employed to give the feed to input straightly.

This pass transistor is regulated by a clock & so it leads to deduction in delay as the data is being transacted. A boost is implied straightly to pass transistors & delay & transaction of data can be made minimal by employing a signal feed by schema. The inverter on second stage is eliminated & the design passes data to from source promptly. The MNX is deployed for two situations to furnish additional driving to node Q while from 0 to 1 transaction of data & discharging node of Q during 1 to 0 on discharging node of Q. additional transistors of NMOS supports feed of signal through a schema [1] & thus deduce the activity of switching.

2.1.3 PROPOSED DESIGN

The input of FF is conveyed to outcome on the falling & rising edge of a clock. The absorption of power is brought down as pass transistor is employed [1]. The data is initiated on both edges respective to deduction to power of clock. The distribution of clock power is the main issue as the given methodology is preferably taken over. This design furnish high efficacy in contrast to triggering on a single edge. Frequency that is required for triggering on dual edge is half of that is put in contrast to triggering on a single edge. The FF that is triggered on dual edge gives greater speed for operation by deducing the delay. It also leads to deduction in area for triggering on both negative & positive edges. It also deduces the sensitivity to pulse noise.

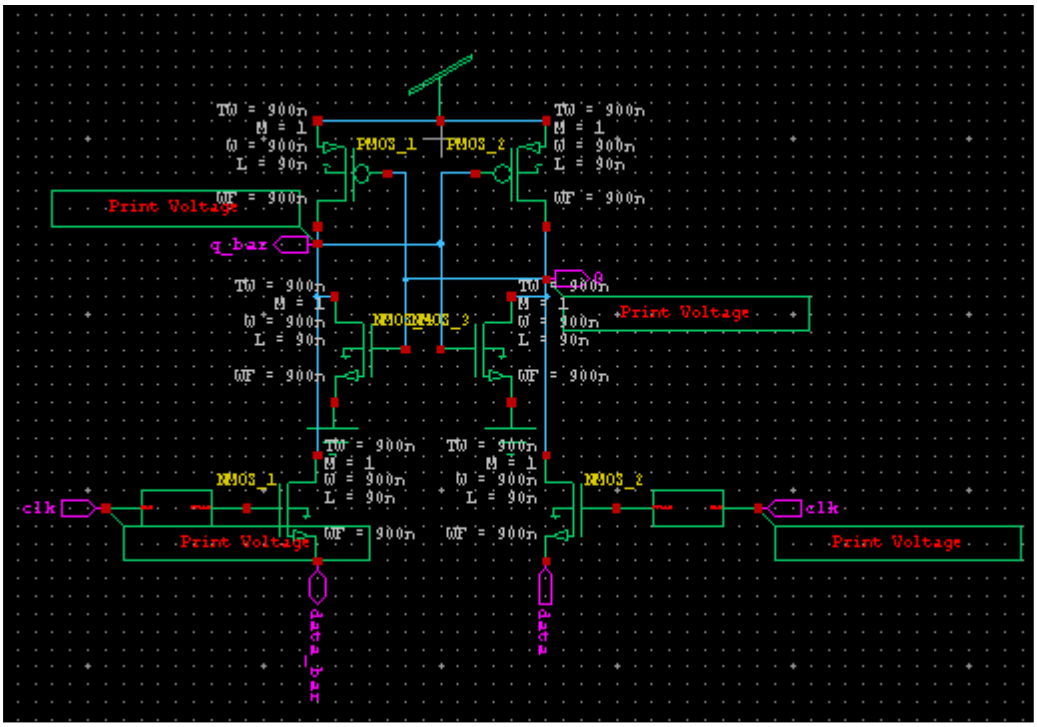


Fig.2.5.double edge triggered flip flop

These inverters instead of NAND logic are used over dual edge triggered FFs. The NMOS intakes input from two sides & a clock is also involved. Inverter initiates information on both falling & rising edges when input is provided. Thus transaction of data works out fast when clock is provided. The design as presented attains greater area as for NAND gate. In suggested design, there is deduction in area when only one inverter is employed. In FFs triggered on single edge, information is initiated on negative or positive edge. It takes several cycles to pass

information. For every pulse generator, NAND gate is employed in present design. This inverter deduces the path of discharging when data gets transmitted from 0 to 1 & vice versa.

DETFFs provide some much better advantages in accordance to need of power & speed. As, data can be transferred over to falling & rising edges of a DET-FF that absorbs very less power. It also leads to deduction of delay when input is provided. By this around 40% of absorption of power can be retained. Even the pass transistor is employed for improvisation in feed signal directly for the deduction in power. In addition to this, DETFF is employed to save power.

Advantages

1:- Deduction in quantity of transistors in stack & raising the leads of charge path to greater speed of operation in contrast to other FFs.

2:- The design triggered on dual edge can work in a minimal voltage & it is best match for the applications that rely on less voltage.

Disadvantages

1:- More absorption of power from suggested design.

2:- Greater delay from suggested design

[2.2] ***In 2013 " LOW POWER DUAL EDGE - TRIGGERED STATIC D FLIP-FLOP " Anurag , International Journal of VLSI design & Communication Systems (VLSICS) Vol.4, No.3, June 2013 DOI*** : This document suggested latest structure of minimal power DETFF which is structurized at CMOS technology of 180nm. In DETFF similar throughput in data is attained with half frequency of clock in contrast to SETFF. In this document, traditional & suggested DETFF are represented & put in contrast at similar situations of simulation. The illustrated outcomes from post layouts reveal that aggregated decadence of power is improvised by 48.17%, 4.29% & 36.84% in contrast to DEPFF, SEDNIFF & SCDFF & improvisations in PDP are 42.44%, 33.88% & 24.69% in contrast to DEPFF, SEDNIFF & SCDFF. Thus suggested design of DETFF is perfectly matched for applications with minimal power & smaller area.

2.2.1 CONVENTIONAL DUAL-EDGE TRIGGERED FLIP-FLOPS

A static output controlled discharge flip flop termed as SCDFF is suggested by M.W. Phyu et.al. SCDFF is ployed in inverters that are cross coupled to retain the information on the outcome. Though the issue faced here is in inverters which are cross coupled that not only bring down the speed of discharging & charging but also leads to short circuits decadence of power. The instance of race current will last long if outcome of load capacitance is greater that may cause distortion in required signals of outcome & also enhance the dynamic dissipation of power. Yan-yun Dai et.al suggested a dynamic explicit pulsed DEPFF. This is required for pre charging the internal nodes & is onto ON PMOS transistors that are deployed in DEPFF circuitries. But it leads to short circuit of current in a scenario where path of discharging is also activated. Xue-Xiang Wu et. Suggested a static explicit pulsed DETFF with latch node incorporated SEDNIFF. [8]. In SEDNIFF, a circuitry on pulse generator is employed to produce narrow pulses on both falling & rising edges on clock as presented in Figure 2.

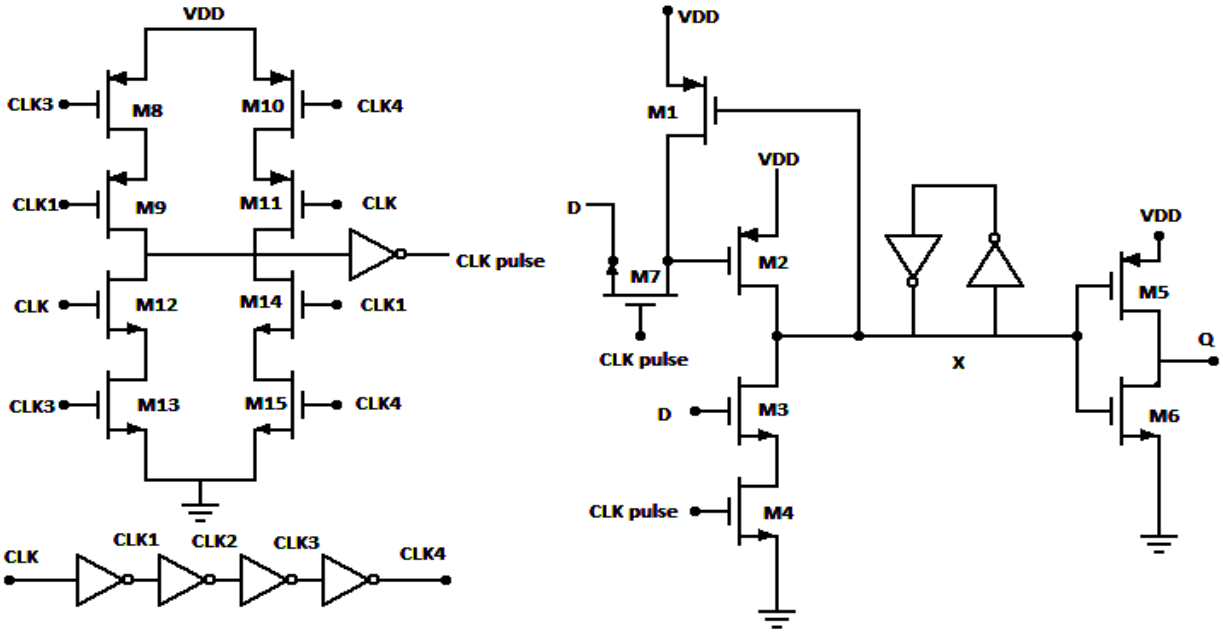


Fig 2.6 - SEDNIFF circuit

In DEDNIGG the charging paths from VDD to CLK pulse are in off state while the discharge paths to ground from CLK pulse are in On state & vice versa. It leads to the deduction in decadence of power in short circuits. Though there are huge quantity of transistors that are clocked are present in circuitry of clock generator, the aggregated decadence of power in the design is more.

2.2.2 PROPOSED DUAL-EDGE TRIGGERED FLIP-FLOP

In the suggested GETFF, the latch of negative & positive state are linked parallel to each other as presented in figure 3. These latches are formulated by making use of one gate of transmission & two inverters are linked joined to each other & outcome from both of the latches is linked as an input to 2:1 Mux. Mux is structurized in a way that by making use of one NMOS & PMOS that are linked in series & gates is even linked to each other & is derived through inverted CLK. Outcome from Mux is linked to inverter to provide strength to outcome. The inverters linked back to back retain the information even when gate for transmission if in Off state & on the same instance, Mux transmits the information latched to inverter to attain the accurate D at the outcome.

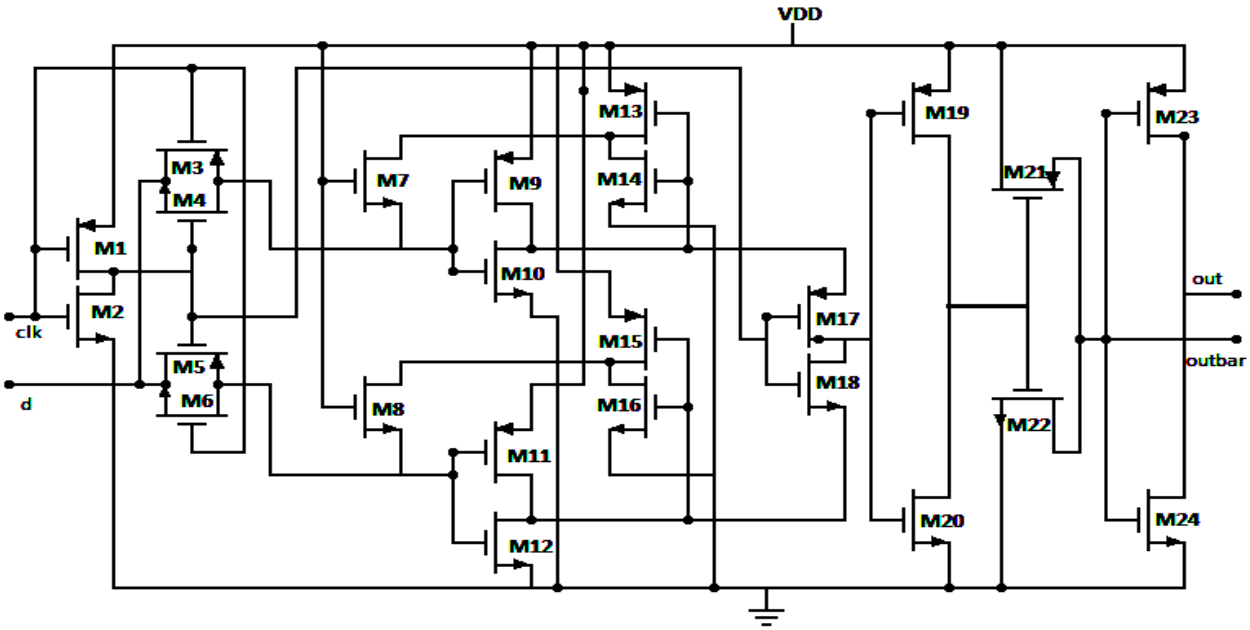


Fig 2.7 - Proposed DETFF Circuit

The suggested DETFF has the working as given below. As CLK is minimal M3, M4 & M 18 are in active state where M5, M6 & M17 are not in active state. As the information is held by negative latch that is lucid to Q. as state of CLK is high M5, M6 & M17 are in active state while M3, M4 & M18 are not active. If value of input D will be same, Q will not be changed. Apart from this, D is transformed before CLK, then D will be held by a positive latch & similar vales

will be transmitted to outcome when CLK varies from Low to High & also for transaction of CLK from high to low.

In this document, we suggest minimal power, area design of DETFF that is static. The suggested DETFF incorporates lessen quantity in accordance to other provided DETFFs. The succeeding outcomes of simulation in the layout experimental state, the DETFF suggests improvisation in decadence of power, power, area & PDP. So the suggested DETFF is the best match for minimal power & applications over smaller area.

Advantages

1:- DETFF attains the equivalent throughput of data in half of the cycle of clock in contrast to SETFF i.e single edge triggered FF.

Disadvantages

1:- Makes use of 180nm technique

2:- More absorption of power.

[2.3] ***In 2014 " Low Power Design of Johnson Counter Using DDFF Featuring Efficient Embedded Logic and Clock Gating " Chandra shekhar kotikalapudi , International Journal of Engineering Research and General Science Volume 2, Issue 5, August-September, 2014***, In this document, we have suggested a design that is power efficient of a 4-bit Johnson counter by employing a DDFF that explains efficient embedded logical module i.e. DDFF-ELM & the clock gating is invaded for deduction in decadence of power. The suggested design ploys a DDFF that s responsible for deduction in decadence of power by abolishing huge capacitances that are accumulated in pre charge nodes of various present designs of FFs by driving the pull down & pull up transistors by succeeding a split dynamic node pattern. This leads to deduction of power to around 40% in contrast to traditional structure of FFs. Then embedded logical module is an effective technique to invade complicated logical functions into a FF. clock gating is implemented for deduction of absorption of power to around 50% because of cardinal activities of clock.

2.3.1 FLIP-FLOP ARCHITECTURES

For the improvisations in the efficacy of FFs to attain greater speed & minimal absorption of power, various structures of FFs are formulated over the decades. All such designs can be incorporated under dynamic & static styles of designs. Static FFs can retain the accumulated information. Static FFs are able to lock retain the accumulated even the clock is not working. There are several topologies of design FFs that were suggested. TGMS & PowerPC 603 slave latch are the illustration of static design styles. TGMS can be incorporated by employing two latches constituted on transmission gates that functions on complementary clocks. Master slave FF PowerPC 603 is amalgamation of TGMS FF & mC2MOS FFs. Main characteristics of these static designs is that they decadence of minimal power & they do possess clock to output delay. As they take greater time for positive setup, static designs accumulate much greater data to delay in outcome. In the designs, if speed is not a much factor of concern designs that are static is the best match. Latest FFs designs that are of high performance are taken under dynamic design style. The designs that are either fully or pseudo dynamic. The design styles for pseudo dynamic are observed as hybrid or semi dynamic as they are comprised of stable outcome & dynamic fronted. The FFs in this class are HLFF & SDFF. HLL is generally a latch that is level sensitive that is clocked with help of a sharp pulse produced internally. This sharp pulse is produced on the positive edge on the clock & is delayed version on clock. The two main producers of SDFF are latch that are level sensitive & a pulse generator. By a sharp pulse that is produced internally which is for short instance, clocking of latch is done so it an act like a FF. Both SDFF & HLFF has gained advantaged from overlapping of clock to execute function of latching. Though HLFF don't have much speed but it is efficient in terms of absorption of power. The logic for slow comparison to SDFF is that HLFF has gained larger stack of transistors of nMOS on the node of outcome. SDFF is considered as the fastest structure that is hybrid as there s much more load on clock & pre charge capacitance is not much effective in terms of absorption of power. In the structured designs that are hybrid, huge pre charge capacitance & redundant data transactions are major source for decadence of power. For eradication of these 2 issues, various structures are suggested & designed. For deduction in the operations that create redundancy in FFs, CDMFF i.e. conditional data mapping FF is the most effective structure. Parallel to this, XCFF is taken as to be the best structure for elimination of huge pre charge capacitances. There are some not required transactions in CDMFF that are abolished by making use of structure of feedback from outcomes to feed the data in a FF conditionally. So, during prediction of a redundant event, this

structure deduces the decadence of power by removing transactions that are not needed. This FF is huge as there are some extra transistors present there in conditions & absorb much more power during more activities of information. Some greater pre charge capacitance in XCFF are presented on the node of outcome that is pulled out by driving outcome pull down & pull up transistors distinctly. There is deduction in absorption of power as one dynamic node from the two nodes is able to be switched during a clock cycle. The main disadvantages of this structure are the sharing of charge & shutoff. The hybrid DDFF abolish the capacitance of large pre charge that is incorporated on the node providing outcome of various traditional designs by succeeding a structure of split dynamic node for driving the pull up & pull down transistors outcomes distinctly. Figure 1 presents stricture of DDFF.

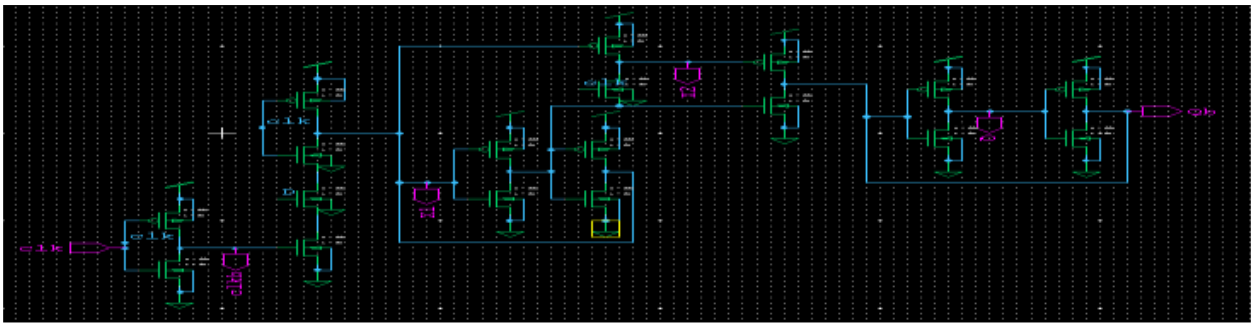


Fig 2.8: DDFF

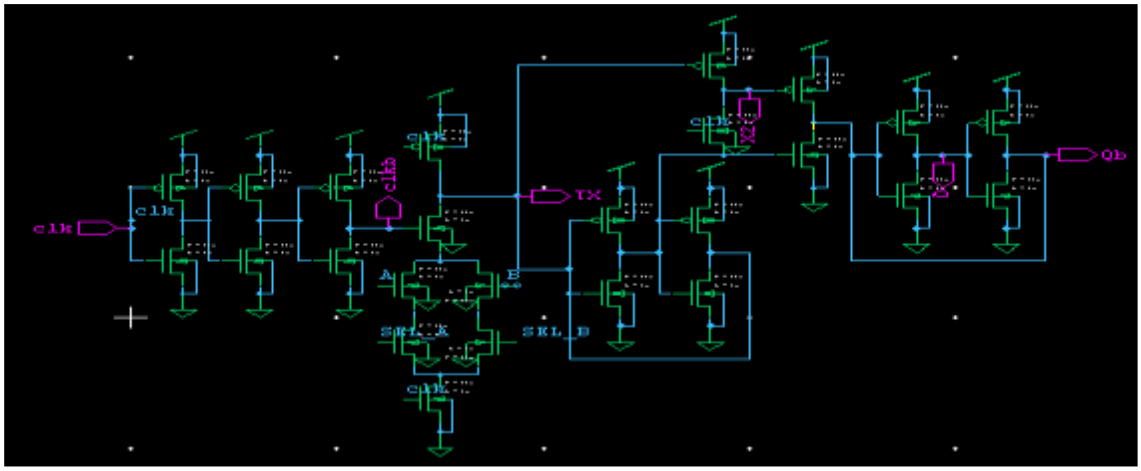


Fig 2.9: DDFF-ELM (MULTIPLEXER)

In structure of DDFF, X node is a pseudo dynamic & even X 2 nodes are dynamic. Irrespective to the mechanism of conditional shutoff, it is presented in XCFF where an unconditional is presented in DDFF. This function is constituted on the state of clock if it is low or high.

Improvisations in performance presents that design of DDFF is best matched for latest deigns with greater performances where decadence of minimal power & delay are needed. Structure of DDFF-ELM is presented in figure 2. Complicated logical functions can be incorporated very efficiently into DDFF structure. The superiorities DDFF-ELM possess over other FFs is that they have logics incorporated into them have minimal absorption of power & can also embed complicated logical functions.

2.3.2 4-BIT UP-DOWN JOHNSON COUNTER

A counter is that device that accumulates the number of occurrence of a process or event in accordance to a clock signal. Counters can be employed in every circuitry of digital formats to count the events. There are several counters that are employed. Johnson counter can also be said as twisted ring counter as it is formed by modifying a ring counter. Figure 3 presents the structure of 4-bit synchronous up down Johnson counter. In Johnson counter, complement of outcome from last level is taken & it is linked to input of the first level.

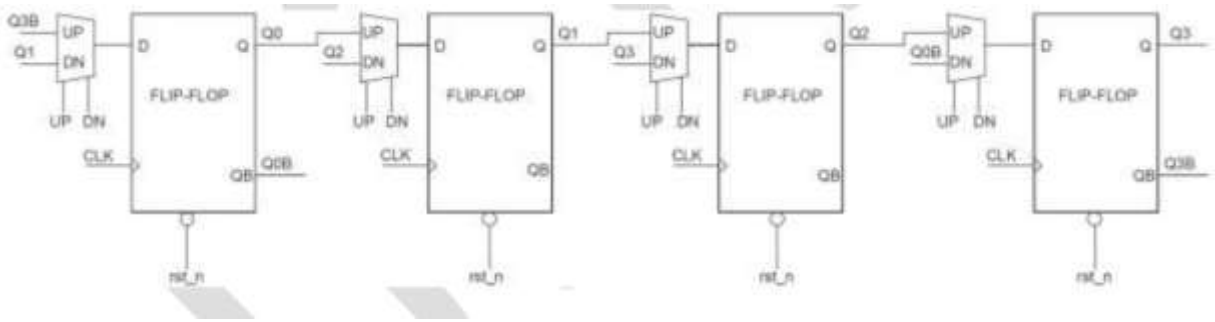


Fig 2.10 :4-bit up-down Johnson counter

In 4-bit Johnson counter, the presented hybrid DDFF is employed. By incorporating a multiplexer into a FF structure is presented in figure 2, where operation of computations is executed in either upward or downward mode of computations. The complement of outcome at last stage & is linked to input of the first level for an up counter & complement of outcome of first stage is find out & is linked to input of last stage as presented in figure 3.

In this document, a hybrid DDFF, an incorporated module of logics, a synchronous 4-bit Johnson Counter & Johnson counter gated on clock are represented. Outcomes of simulation present improvisations in speed & power. The hybrid DDFF presents improvisation over cross charge control FF i.e. XCFF as it abolish the decadence of redundant power. Further to this, complicated functions of logics can be involved very efficiently in a FF. A 4-bit Johnson counter with gating

of clock reveals improvisation of power of around 50% in contrast to the 4 bit up & down counter with no gating of clocks even the area is increased. So, in latest designs with greater performance where absorption of power is the main point to be taken care, the structure as presented is the best match to it.

Advantages

1:- The design as suggested incorporates a DDFF that deduces the absorption of power by abolishing the greater capacitances that are involved in pre charge node of various present designs of FFs by forwarding the pull down & pull down outcome distinctly by succeeding a structure of split dynamic node.

Disadvantages

1:- More absorption of power from our suggested design.

CHAPTER 3

PROPOSED DESIGN

3.1 DOUBLE EDGE TRIGGERED FLIP-FLOPS

We observed the earlier structure of DEFF & segregated them into 3 parts: traditional DEFF, DEFF as explicit pulse & DEFF as implicit pulse. The schema for formulation of pulse of clock is assessed as well schema for combining the data. Design of DEFF will make use of many other transistors which are clocked than the design of SEFF. Since the design of DEFF must not be raised by load on clock. The goal of design of DEFF must be to save the energy on networks that are distributed & FFs. It is given preference to minimize load on clocks of circuitry by lessening quantity of transistors that are clocked. Further there will be a deduction in activity of switching that will be deduced & preferred. The capabilities of minimal switching will be supportive on distribution on network of clocks in terms to save the power. As by a fact that scaling of voltage can lead to deduction in power systems like CVS have gain much popularity. These points to those FFs that have capability to transform the level can be deployed in these conditions. So amalgamation of FFs & shifter of level is much supportive in this scenario.

3.2 CONVENTIONAL MASTER–SLAVE DOUBLE-EDGE TRIGGERED FLIP-FLOP

A basic schema is presented in fig 3.1. A traditional method to formulate the DEFF is copying the portion of latching to a FF having one edge to attain sample data input at both the edges of clock. This eventually doubles area & also enhance load on inputs of clock & data that puts an impact on performance. This puts an adverse impact on gains that are retained that will half the frequency of clock on network that is distributed. An illustration of a traditional FF od DE is presented in Fig 2. Left hand side do sampling of data as clk =1 & right side sample date as clk=1. The path of data will be copied.

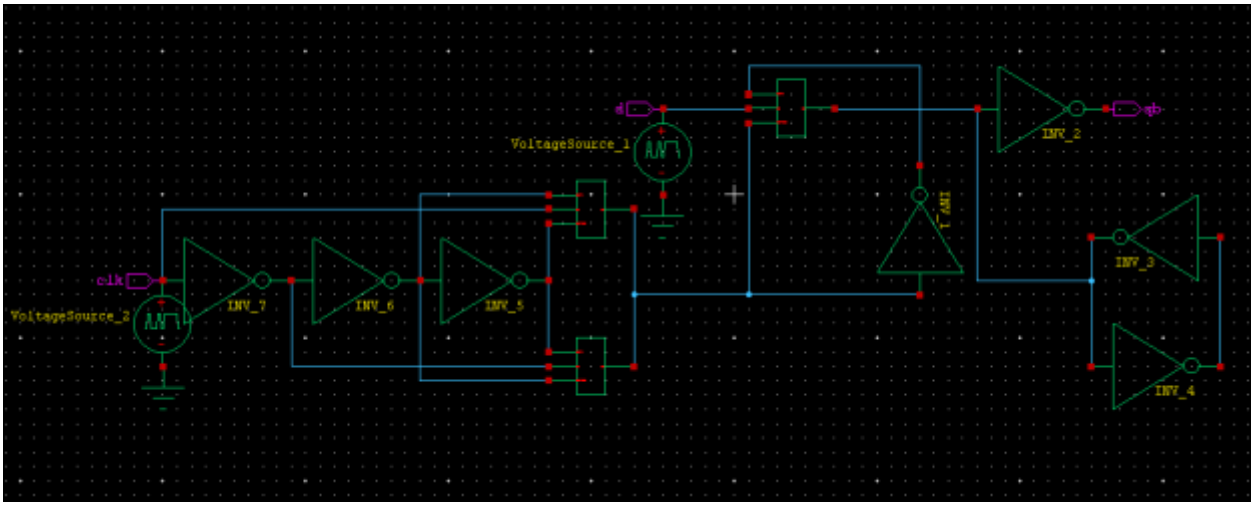


Fig 3.1 :- Master–Slave Double-Edge Triggered Flip-Flop

3.3 FLIP-FLOPS WITH EXPLICIT PULSE GENERATOR SCHEMES

The FFs on condition of master & slave has properties on hard edges. FFs of pulse permits stealing of cycles & possess tolerance to skews. DEFFs that are explicit make use of a generator of pulse that is outbound to area of latching & don't need any copying. A basic schema is presented in figure 3. The formulator of pulse of double edge can be assumed as XOR that makes use of an inverter which is floating, a XOR that makes use of transistors of pass or a XOR that makes use of schema of transmission. The portion of latch can be gate of transmission, TSPC SPLIT, PASS or others. This structure has a transparent window by a pulse that is formulated explicitly. The formulator of pulse is constituted on TG & logics of XOR. There is a basic design on a sensitive complicated way so load on capacitance may be minimal.

Though it possess an input of diffusion that is exposed that is related to noise & there is proportion of ep-DSFF. There may be an addition to TG3 input for improvisation of capabilities of driving & robustness.

3.4 DOUBLE-EDGE CONDITIONAL PRECHARGE FLIP-FLOP

The execution of terminologies of precharing on conditions is impaired to DECPFF. For a feedback signal, Q is deployed for regulation of precharging & deduction in switching on redundancy. As Dis 1 & so Q is 1 which cuts off the path of precharge as it turn off P1. It makes use of schema of duplication of branches that is clocked.

The transistors that are clocked on NMOS on initial branch have same composition as transistors of NMOS which are clocked on proceeding branches. Both branches of transistors of NMOS have identical clocks though their functioning is different. As architecture of clocking is complicated & there are lots of transistors that are deployed to switch clock, advantage to deduce redundant activity of switching has been offset by huge power of clocking. As, there are 16 transistors that are clocked in SPGFF.

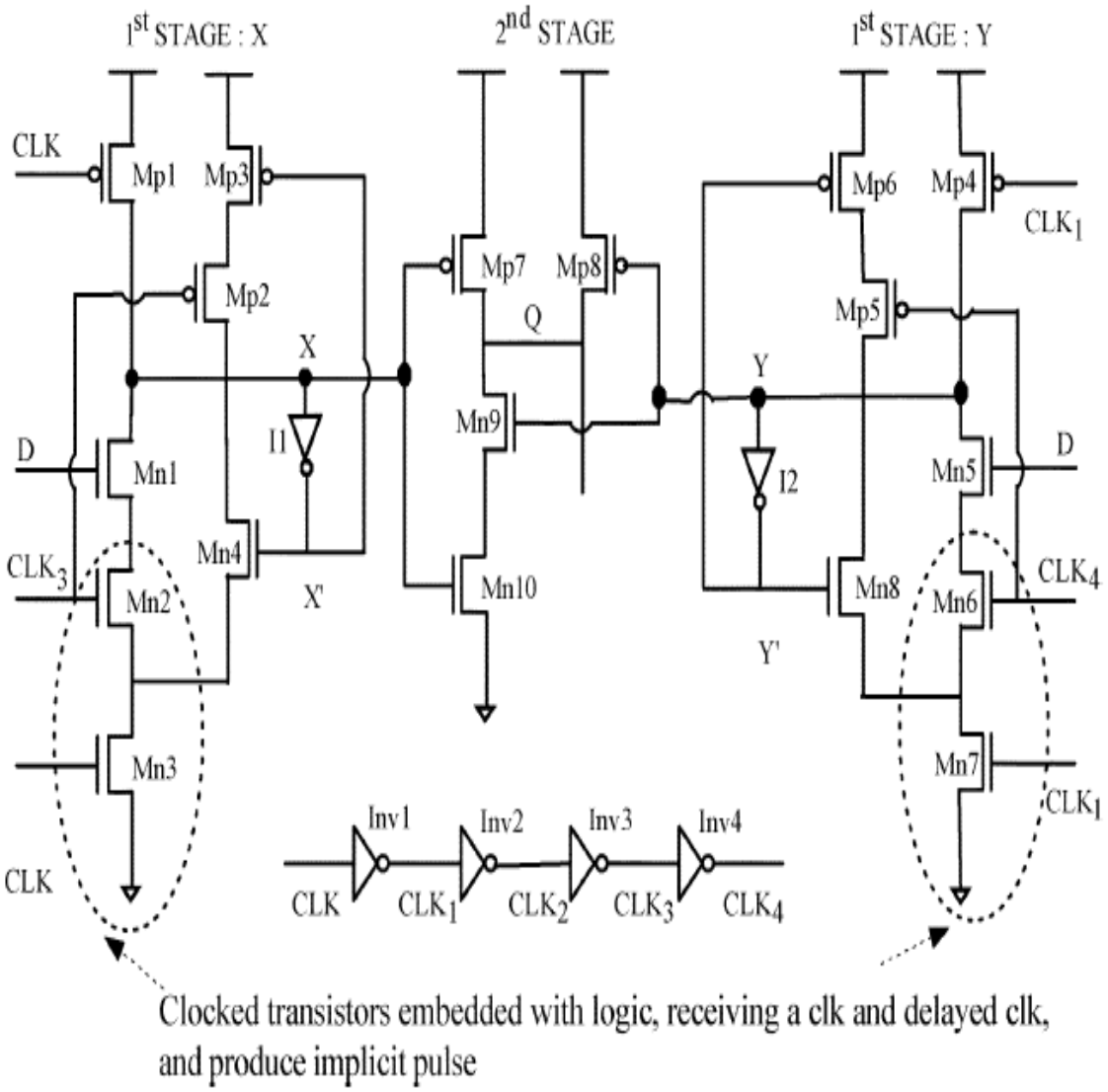


Fig. 3.2 . Symmetric pulse generator flip-flop (SPGFF), total of 32 transistors including 16 clocked transistors.

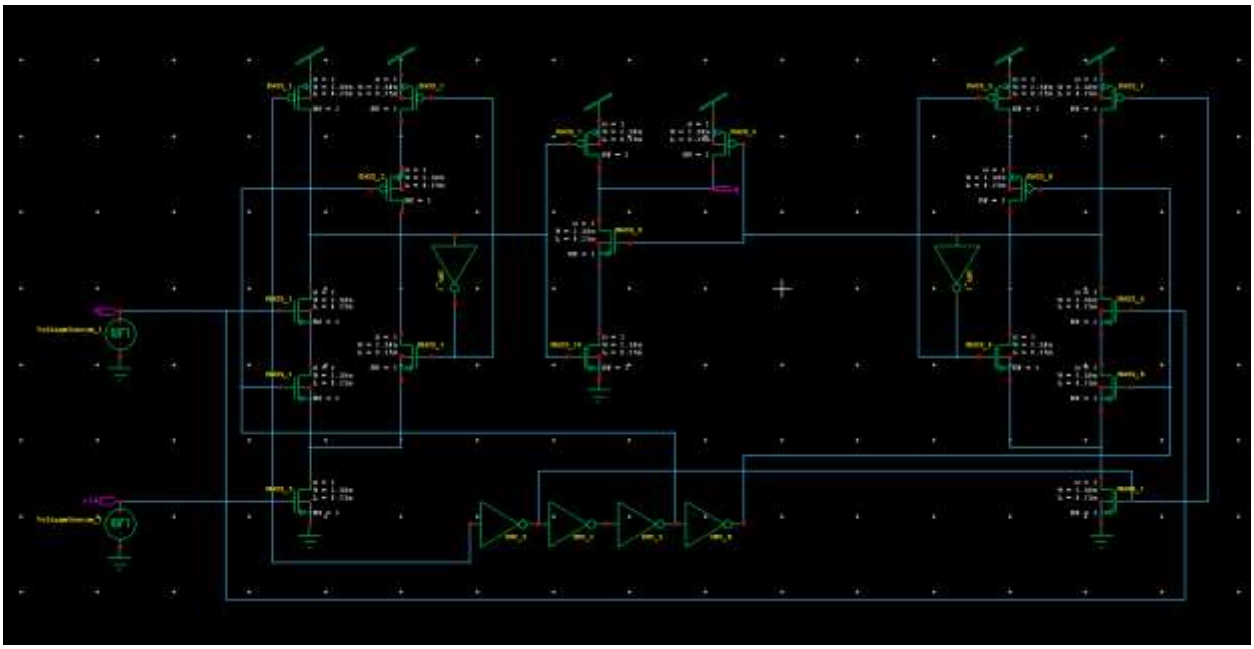


Fig 3.3 :- Symmetric pulse generator flip-flop (SPGFF) CMOS design

There are 21 transistors that are clocked in DECPFF & total transistors are 33 in this. This complicated architecture & huge quantity of transistors that are clocking raise load on clocks & absorption of power. In a manner for implementation of clocking on double edges, SPGGF makes use of 5 transistors that are clocked which are less than that of DECPFF & so in is more efficient.

3.5 PROBLEM STATEMENT

A FF with minimal power & dual edged is suggested that is constituted on feed of signal. Absorption of power is the main concern in design of circuitry. In present circuitries DEFF & SPGFF intake much transistors. This is the cause for raise in absorption of power. As it can be observed from design of circuitries on pictures, both have more than 10 transistors in them. So absorption of power is more even than the circuit as suggested. He delay will be more with increase in area. This leads to a major concern in structure of VLSI circuitries.

3.6 PROPOSED METHODLOGY

For deduction in terms of delay & power in present circuitries, quantity of transistors is brought down. As per the image 3.4, transistors are very much less than present circuitry. The traditional DEFFs copy area & load it onto inputs. Pulses that are explicit in DEFFs make use of outer generators of pulse of clock that enhance power in circuit. Summing up to this, outer pulse of DEFFs doesn't work with logics that are dynamic. SPGFF makes use of implicit pulses so it has nodes of switching which are four in number & are implicit. Not like to SPGFF, DECPFF gets rid off the activities of switching that are redundant even the quantity of transistors becomes 21 & copied architecture of branch of clocking is complicated. For assurance of execution of a clock of double edge that that triggers in an environment having a pulse that is implicit to come over with the issues with lastly FFs that are implicitly pulsed which has a big load on clock, a topology of sharing of branch of clock is suggested.

This system of sharing is like to clock FF having only one transistor & other FFs that has branch of a clock. In this schema as in fig. 3.4, two sets of branches that are clocked in last branch of clock segregates the schema which are amalgamated; were Ni, N3 & N2, N4 are being shared by 1^{st} & 2^{nd} level. It is noted that a path that is split is provided for assurance of satisfactory working even after their amalgamation. Superiority this concept proposes is to bring down the quantity of transistors for implementation of branches of clock over triggered double edge FFs having implicit pulses. By not sharing quantity of transistors which are clocked can be greater than that of concept of sharing. It is observed that transistors that are clocked possess a factor of activity of 100% & absorb most of the power. By deducing transistors, power can be minimized in a better way. Implementing faked NMOS in CBS_ip, it gains that D & Qb possess polarity on inverse that results from methodology of discharge based on conditions. The way of discharge remains in active state only for a short instance furnishing lessen current in short circuitries. Isolation from coupling by noise is done by implementing inverter in front.

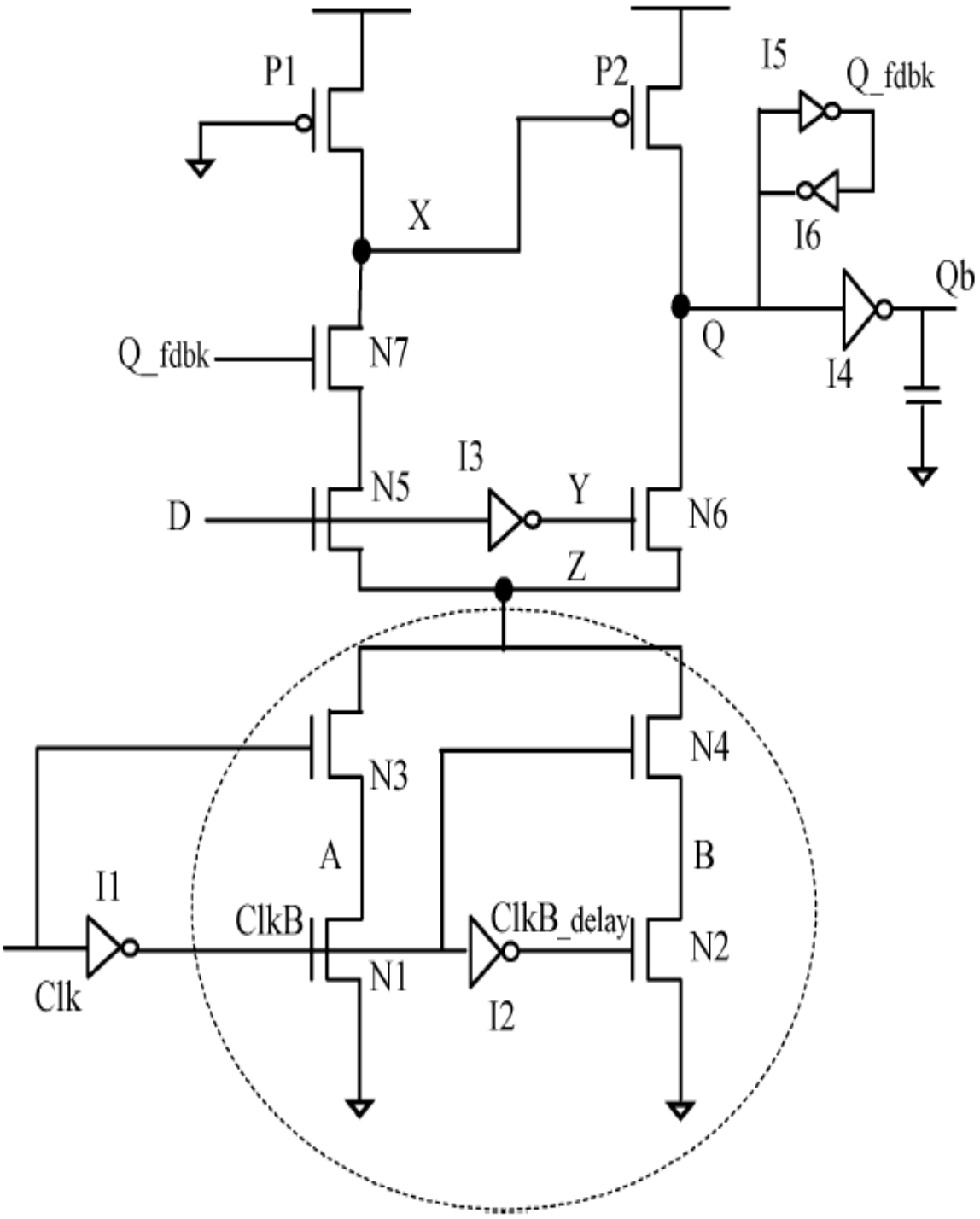


Fig 3.4 :- Suggested FF of CBS-ip

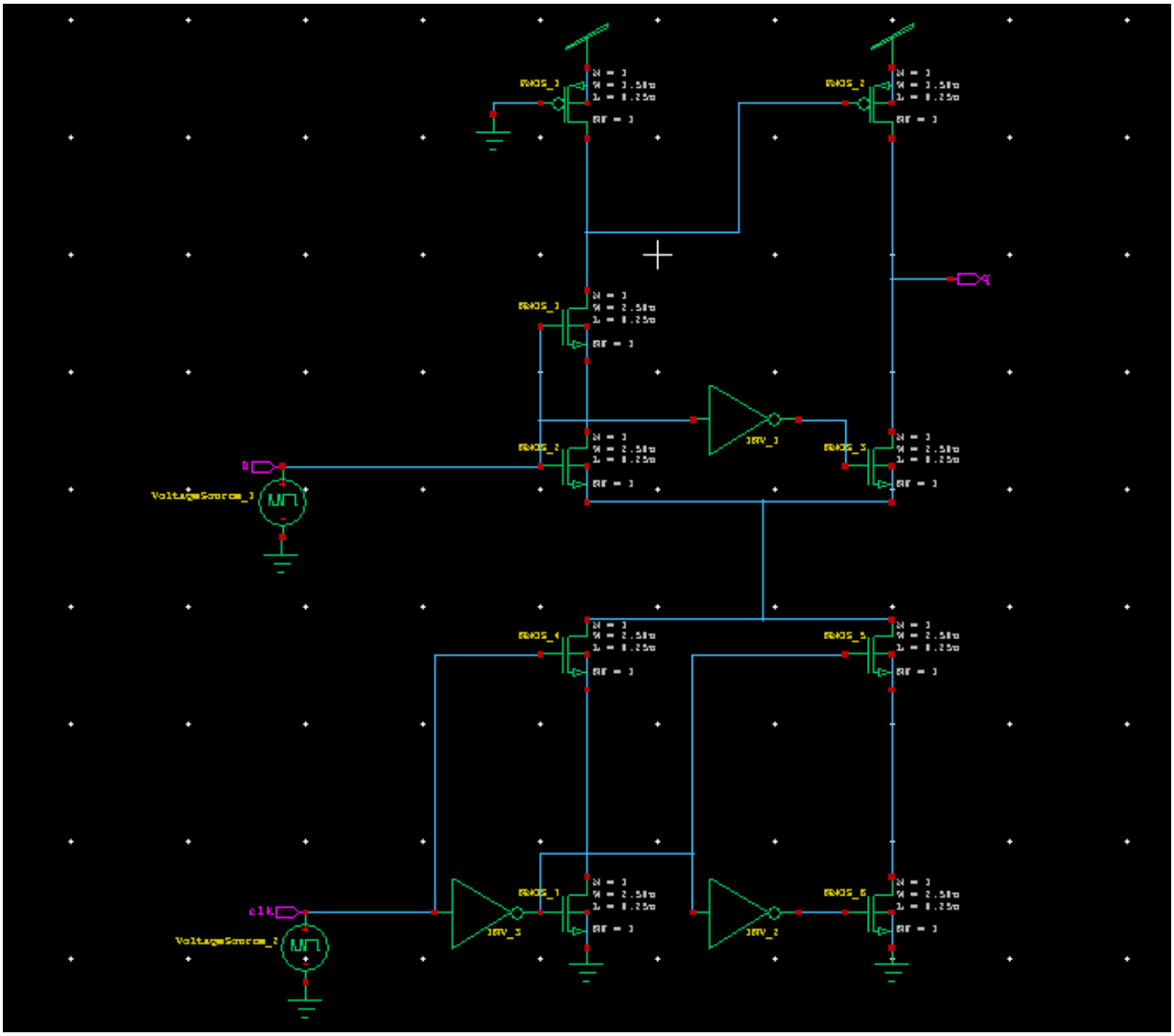


Fig 3.5:- Suggested design of CMOS in FF of CBS-ip

3.7 INTRODUCTION TO TANNER TOOL

It is in general an assessment program of Spics determined for circuitries which are analog. It has the machines given below:

1. S-EDIT
2. T-EDIT
3. W-EDIT
4. L-EDIT

By implementing such sort of driving instruments, a facilitation is gestured by spice program make use of the provided blueprint & imitate dome new formulations in the analog ICs rather than giving a thought to procedure to formulate a chip that is much expensive & consumption of time.

3.8 SCHEMATIC EDIT TOOL (S-EDIT)

As a collection, it is a set of modules, pages & portfolio. It gives an induction to token & modes in diagrams. S-Edit facilitates the following:

1. Commencement of design.
2. To visualize, edit & draw objects.
3. Linking associated to design.
4. Lists of net, simulation & components.
5. Schema of browser, mode of symbol & instance.

Commencement of design: It gives a detailed explanation about the procedural of design constituting module & operation of file.

Browser: For an efficient design of schema the information of operation of S-Edit hierarchy that is formulated of tokens & sections are necessary. The outlines of S-Edit are constituted in modules. The module is the prime constituent of the appliances like gate, amplifier & transistor.

There are two proportions of a module:

1) Primitives: Calculus objectified as portrayal tools.

2) Occurrences: Indication to other portions of file. The real module is at an instance.

There are two ways to view an S-Edit:

1. Mode of Schema: It is deployed to look over the schema or formulate a new one.

2. Mode of Symbol: A unit that possesses greater functionalities is presented by the given mode.

3.9 T-SPICE PRO CIRCUIT ANALYSIS

The visualization on the assessment of integral elements of the circuitry of T-Spice pro is

described as:

.sdb: it gives explanation of the circuitry by way of manipulation & assessment by deploying S-Edit.

Input files of simulation with extension (.sp): scrutiny in textual form is described by this circuit, for purpose of editing & T- Spice Simulator for Circuit possesses simulation.

End product files of simulation (.out): it contains the numerical results of the circuit analysis, required by Viewer of W- Edit Waveform for display & manipulation.

3.10 CIRCUIT SIMULATOR (T-SPICE)

The exploring feature of waveform of T-Spice integrates S-Edit, T-Spice & W-Edit that allow a single level of circuitry that is explained & assessed. Some assessments are given as:

The input file is the center of T-Spice operation. It is also called to be as the elucidation of circuit, the total list & the deck of input. It is the simplest file that retains the data related to the statement of device & commands of simulation that is exaggerated by the simulation of Spice by which assistance T-Spice formulates a dummy that is imitated. The files of input can be formulated & manipulated by an editor that edits text.

A tool that is needed to simulate the circuitry is termed as T-Spice. Its main facilitations are:

1. Commands of simulation
2. Simulation of design
3. Statements of device
4. Model of noise & low signals
5. Models designed by user & external

It implies KCL to find out an optimal solution for circuitry. The circuitry of this is a network of nodes which are interlinked to each other with voltage presented at every single node.

T-Spice first solves equation for the voltage at a node that satisfies the condition of KCL considering that total amount of current flowing in every node will be net neutral. The computers formulated on this machine sums up the current that comes out of the every single device that is linked to the nodes & the extremities to assess if the voltage at the node is an appropriate answer

to this issue that is being faced.

The following equation determines the derives a link in the current & voltage induced at the extremities in the appliance with the resistance R: $I=\Delta V/R$ & ΔV is ployed to present difference in voltage. Some of the out produced results are discussed below:

3.11 DC OPERATING POINT ANALYSIS

It is applied to find the state of steadiness of a circuitry that is invaded as the voltage of the input is implied for a particular time. T spice accumulated .include that will gain & read constituents of a standard file to assess the transistors NMOS & PMOS.

The model criterion for p-type and n-type device the file of techs figures are being allocated to MOSFET by the file of technology. These parameters are made to use to appraise correspondence of MOSFET, and the results obtained from it were deployed to formulate the internal tables of charges & current when it is being picked out by an input file. The values of these tables are implied in the calculations of simulation.

Following each transistor the name given to them are taken as the names of the terminals. The needed organization of names of terminal is: gate, drain, loft & source. By furtherance names NMOS and PMOS given as an illustration with the specification of their physical attributes. The function of .op is of calculating the DC point operation & rewrites the assessed outcomes to the given paper in the dialogue of simulation. The description of circuitry as by the input file is being listed as the DC operating point information by the paper of outcome.

3.12 DC TRANSFER ANALYSIS

The need of it is to commence a theory of the current r either voltage at one node out of the several provided nodes which is accounted as function of current or voltage with the nodes linked to it. It is determined by brushing the variables of the source in a set domain with the outcome that is tracked. The command of .dc operated the list of sources that are required to wiped away & domain of voltage by which the switching needed to be deployed and also pointing towards the assessment of transfer. The deployment of assessment of transfer will be as: the deployment of vdd at 5V & switching of vin in a particular domain over a particular domain; the vdd will be incremented this way & the again switching if vin will be performed over a domain that is defined & it goes on this process will be carried on till the peak of the domain is attained by vdd. In eneral,

the values which are then accumulated to the voltage sources vdd and vin are ignored by .dc command in the voltage source statements but its mandatory to declare them in those statements. The .print dc command is used for reporting the results for nodes in and out to the particularized destination.

Assessment of Transient

In informs about fluctuations in elements of circuitries in accordance to time. There are 3 standard modes for command of T-Spice for assessment of transient. In the standard mode, the functional point of DC is found & the commencing point for simulation of transient. The command of .tran exhibits the characteristics of assessment of transient that is to be executed.

3.13 AC ANALYSIS

The assessment of AC reveals the conduct of dependence of circuitry on the frequencies of small inputs. There are three phases of it: (1) computation of point of operation of DC; (2) linearization of circuitry; (3) need of linearization of every circuitry. As source of voltage of ac is to be appealed, then difference of voltage determines the voltage gap of DC in node as minimum as -0.0007 volts, the AC has 1 V magnitude & phase of AC is 180 degree. Assessment of AC is performed by .ac command. The information that bothers the frequencies meant to be swept while during the analysis is operated by the .ac keyword. In a scenario where frequency has to be switched as logical manner by DEC, by each decade 5 nodes of data are invaded to it. The enjoin of .print pick up the default unit as decibel for the voltage magnitude and degrees for the phase and write it down into a file particularly. The command of .ac observes the attributes of small signals & also the operational current & voltages for the circuitry.

3.14 NOISE ANALYSIS

There is isolation of actual circuitries from fluctuating variations in terms of voltage & levels of currents. The effect that noise put is determined & conjunctively reported with assessment of AC is T-spice. The actual reason for assessment of noise is to find the effect of noise in accordance to variegated circuitries on out produced voltage by means of frequency function. The assessment of noise is determined by incorporating assessments of AC to it. If by any means, the command of AC is not over there, then command of noise is left as such. The function of .noise command will be executed only if .ac command is there at similar level of frequency. There are 2 factors that are

considered in command of .noise, the outcome required to calculate impact of noise & input value where .noise is taken as focused to determine density of spectrum as being equivalent. The command of print is taken as to print the outcomes.

3.15 WAVEFORM EDIT

This Edit is taken as ability to present complicated data in numbers that leads to simulation of circuitry & is much hard to get to test, improvisation. It is basically viewer for waveform that is easy to implement; power up & speed in an environment which is flexible particularly for presentation of data in graphs. The supremacy of this incorporates:

1. a fine regulation of Tanner EDA & T-spice simulator deployed in the circuitry. The information can be edited in the format of charts that is produced by the T-Spice with no manipulations in the files of the data out produced. This information may be manipulated in the files of the informatory texts of outcome. This information may be represented in the form of charts dynamically as long as it is generated while the process of simulation works.

2. Charts can be regulated as such by the form of data.

3. A unit called as trace is determined by this. There are several traces that on grouping formulate several files of outcome which can be seen as in several or single window. There are several copies of these traces formulated & shifted among various charts & windows. Arithematic of trace is executed on the ongoing tracing.

4. The views of charts can be shifted in any direction, may be zoomed in & out by providing the definite co-ordinates in axis of X & Y.

5. The attributes of charts, axes, rides, colors etc can be manipulated as per the requirement of them.

The input is furnished in the form of numbers to the W-Edit. For automatic chart configuration, Header & Comment information is used which is provided by T-Spice. By association of T-Spice which is functioning with W-Edit, a runtime update of output results is made possible. The data is retained along the transcends, coordinates, charts in W-Edit in a database which is abbreviated as WDB.

3.16 LAYOUT(L-EDIT)

The tool that visualizes the subjects that formulate an integral circuitry is termed as L-Edit. It terms the formation of design in the terms of cell, primitives & files. The terminologies of the constituents don't comply on the stage of schema of layout level. Thus it is used to facilitate the user to determine first the how the circuit responds past to transfer it to next stage with the time that is required along the price. Some key points are mentioned here to formulate a fine layout of the schema of a circuitry which can be later on implied as user to put in a comparison with the response of output with the one which is expected.

3.17 L- EDIT: AN INTEGRATED CIRCUIT LAYOUT TOOL

The tool that visualizes the subjects that formulate an integral circuitry is termed as L-Edit. It terms the formation of design in the terms of cell, primitives & files. Any required quantity of files can be retained in the storage. There may be the desired number of cells in every single file. The provided files may have no connection to each other or hierarchically related like in a typical design like a file in library. Any number of adjoined masks & cells may be retained in the cells.

Cells: The standard blocks for building.

Cells are taken as main constituent of a circuitry. The layout of design comes up in the cells. The cell may be:

- Incorporates partial or whole design.
- Can be taken as reference for other cells.
- Can be formulated by instances of various cells.
- Incorporates real formulated objects.
- Can be formulated by whole primitive or amalgamating primitives & instances of cells.

3.18 HIERARCHY

It furnishes support to complete hierarchy of mask. Cells may incorporate various instances. An instance is taken as a mark for a cell which is not linked, if a change is edited that will be presented in every instance of cell. The instances are needed to formulate updating process & making it much simpler & they bring down the need of storage of information as no requirement is there to retain the data furnished in the cell that is instanced by a reference to the cell will be

sufficient by the data positioned on instance, which is retained in it briefing about the mirroring & rotation of it.

No distinct network is deployed for L-Edit. Though primeval & occurrences may be retained in the same block of this topology. The files consisting of design are self constituted. A pointer is set that will always point to a cell within the same file containing design at an instance. When a replica of a file is formed, some replicas are diversely formulated by L-Edit, to signify the self continence of terminal.

3.19 DESIGN RULES

The regulations on manufacturing can be exhibited in L-Edit like rules of designs. The evaluation of layouts can be done against these.

3.20 DESIGN FEATURES

The editor is also been counted in L-Edit which can be manipulated as per the need. The layout operated in a manual way may be possibly attained a bit fast as L-Edit possess an interface which is friendly to users. Adding up to this there is no worry about the issues observed in variations that are automated. By illustrations, bars of guards, Phototransistors, transistors with dual polarity are termed as horizontal & vertical, figures which are static, & diodes of shottkey that gives much leniency to the optimized designs of technology of CMOS being the normal transistors of MOS.

3.21 FLOOR PLANS

A tool to create plans is also constituted to L-Edit which is manual in nature. There is a choice among the instances to display in an outline which can be recognized by a geometry that is fledged or by name. The arrangements of the cells in the design can be manipulated quickly & easily when the outline of design is represented in order to accumulate the planning of floor. The occurrences in the topology can be refreshed at any stage which can be lied in a hidden position or visualized as it is required my applying some graphics or functions which are rotational guidelines that can be deployed on geometry of mask that is primary.

3.22 MEMORY LIMITS

The files of designs in L-Edit can be formulated as per greater wish in the provided RAM & storage.

3.23 HARD COPY

The hard print of design can be done by L-Edit. An option is that allows to choice to take print outs of greater plots on a defined scale. Macro is there to furnish support to high ended large sized plotters to do plotting in colors.

Variable Grid

The choices of grid in L-EDIT give assistance to designs formulated on lambda along with the design based on micron & mil.

Error Recovery

The mechanism of tapping of errors in L-Edit identifies flaws in system particularly & in many scenarios in furnishes a way for recovery of information without any loss.

3.24L- EDIT MODULES

- L- Edit : it is the editor of layout
- L- Edit picks an extractor
- DRC of L- Edit: it identifies the rules of design

An editor of mask that has greater throughput, features & user friendly is L-Edit. The layouts formulated by it are very quick & simple & assists the hierarchy, permitting the number of layouts that as much as needed. It is constituted by the major portions & allows using all modes of angles. The lists of net from the layouts of circuitries of Spice are formulated by extract L-Edit which recognized as devices which are active & passive, sub circuits, and the commonly used device attributes incorporates capacitance, length of device, resistance, area & width of device, source & drain area.

The attributes of DRC of L-Edit are the regulations that are customized by user & find out which is minimal surround, not any existence, overlapping, & the regulations of extension. In can regulate the whole chip & portion of DRC. The flaws of browser * functions of objects for swift procedure to recycle are provided by DRC for checking of regulations.

CHAPTER 4

RESULTS & SIMULATION

4.1 EXISTING DESIGN

4.1.1 CONVENTIONAL DUAL-EDGE FLIP-FLOP

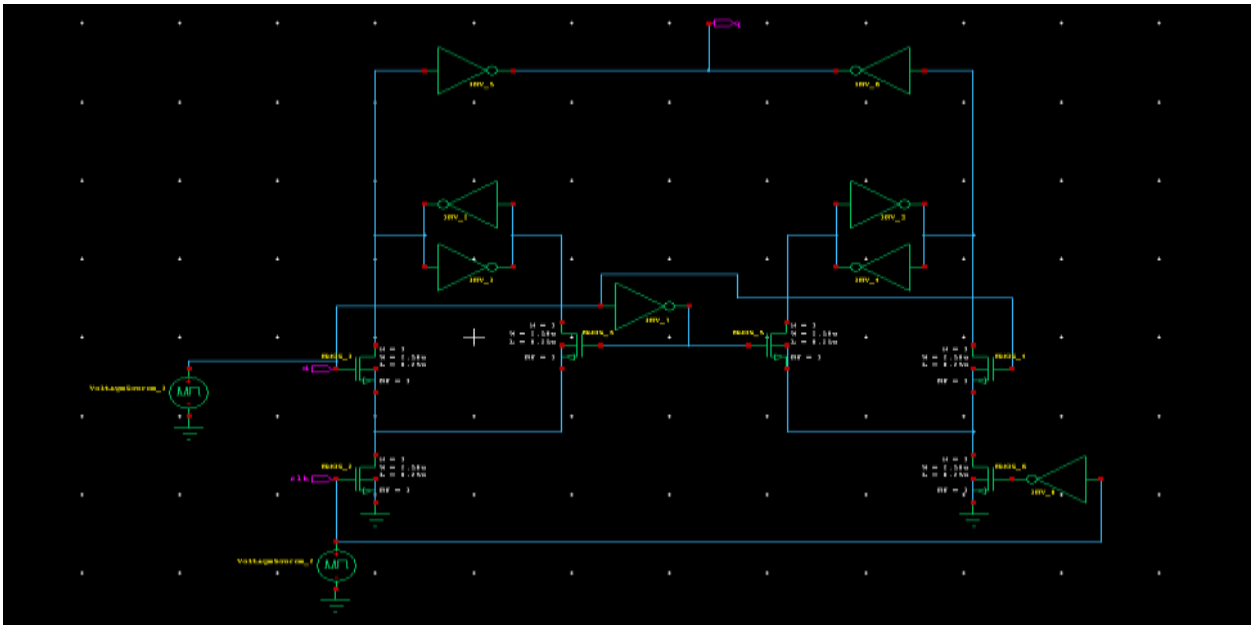


Fig 4.1 :- Design of CMOS for traditional FF of dual edge

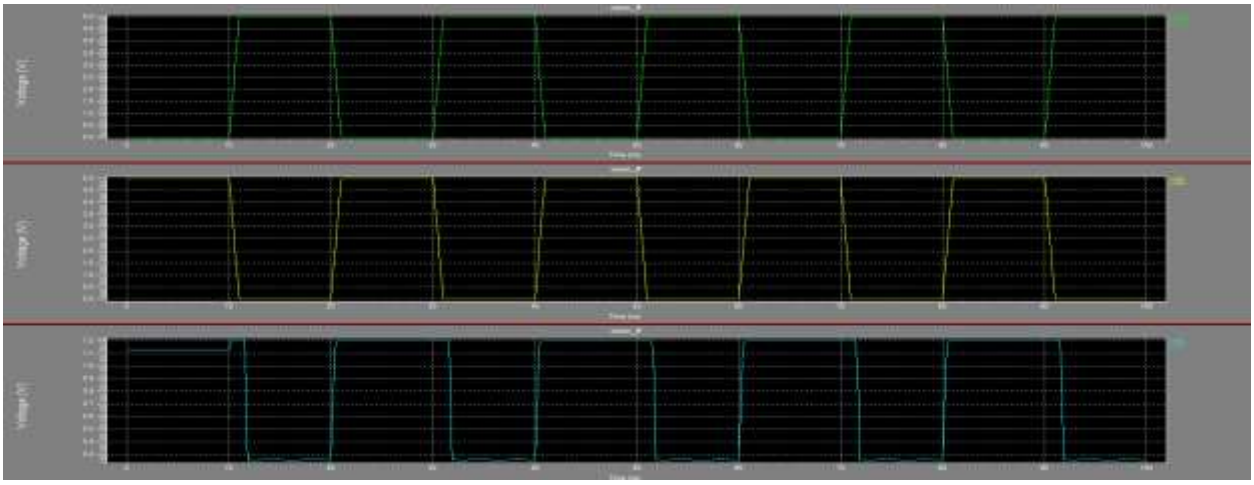


Fig 4.2 :- Waveform for traditional FF of dual edge

Traditional FF of dual edge is a design by 45nm file of tanner. Length of channel for this designed circuitry is 45nm. Absorption of power by outcome for traditional FF of dual edge is 3.308421e-004W.

4.2 DUAL-EDGE STATIC HYBRID FLIP-FLOP

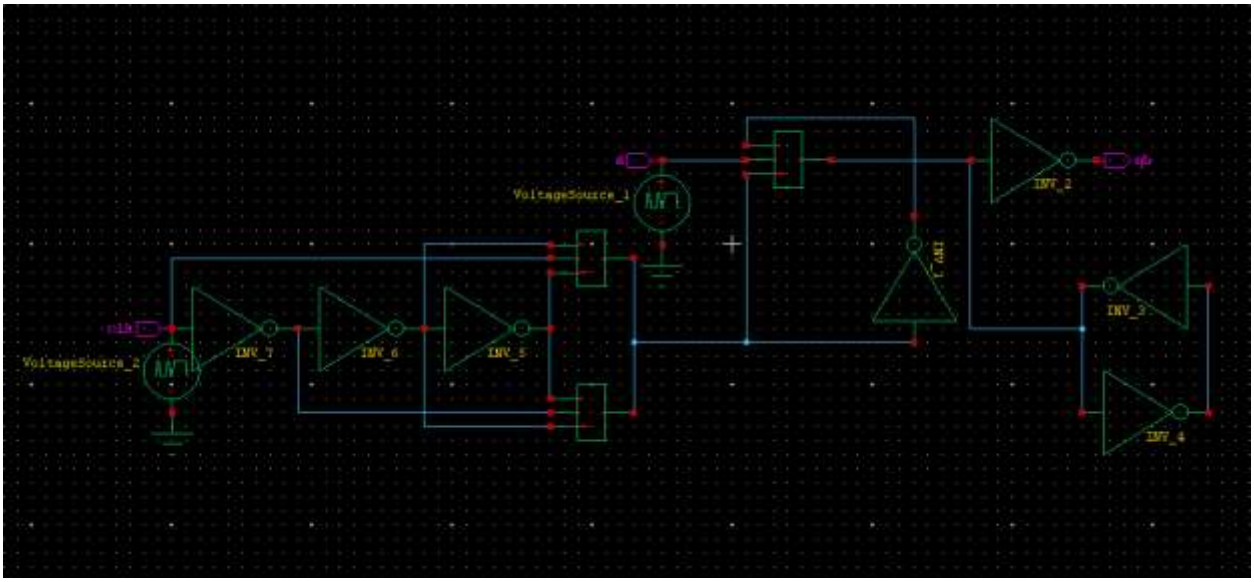


Fig 4.2 :- Design of CMOS for FF of dual edge

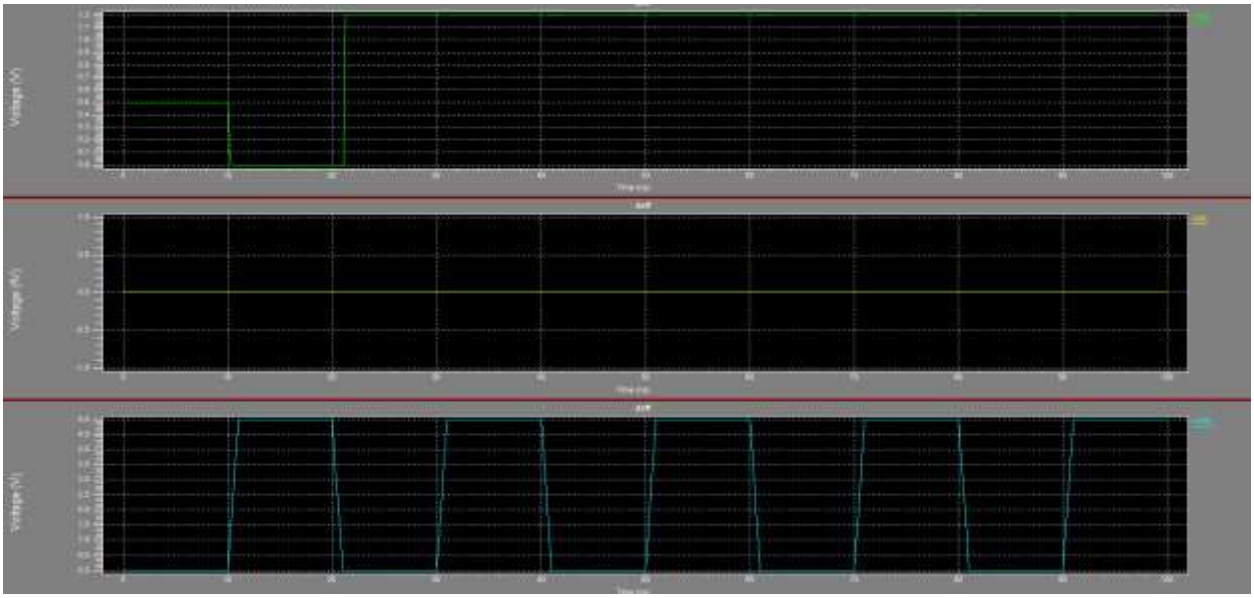


Fig 4.3 :- Waveform of outcome

The power consumption for the Dual edge flip flop is 1.693103e-004 watts .

4.3 SYMMETRIC PULSE GENERATOR FLIP-FLOP (SPGFF)

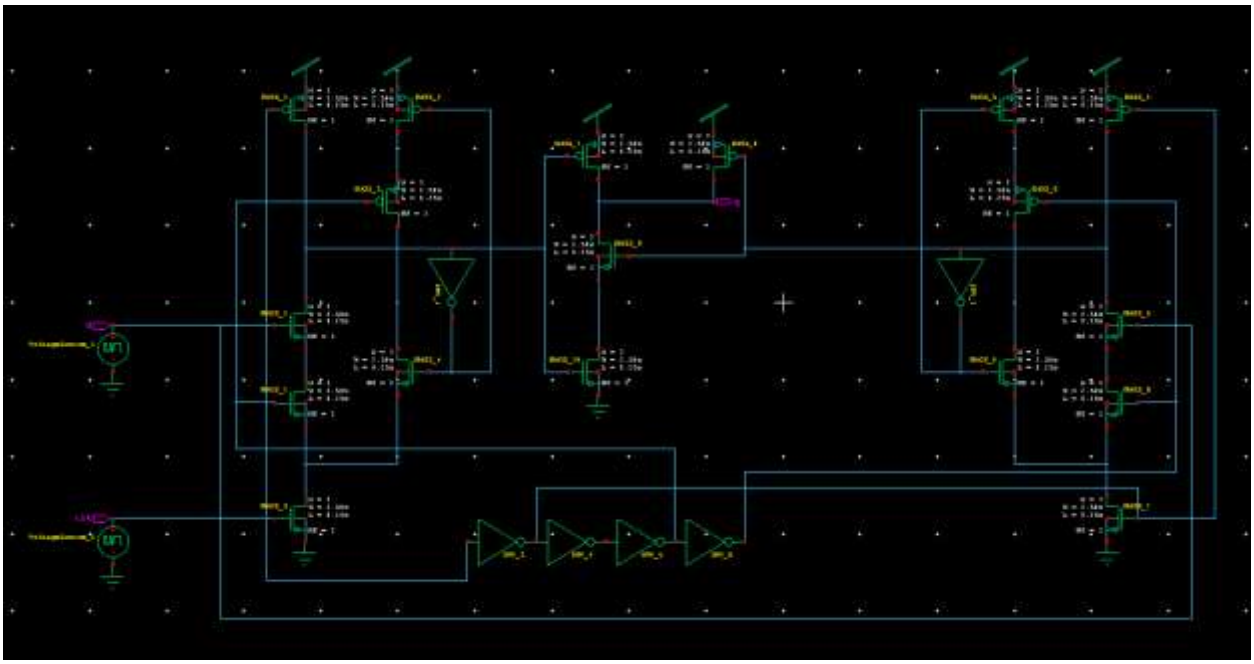


Fig 4.4 :- CMOS design for Symmetric pulse generator flip-flop

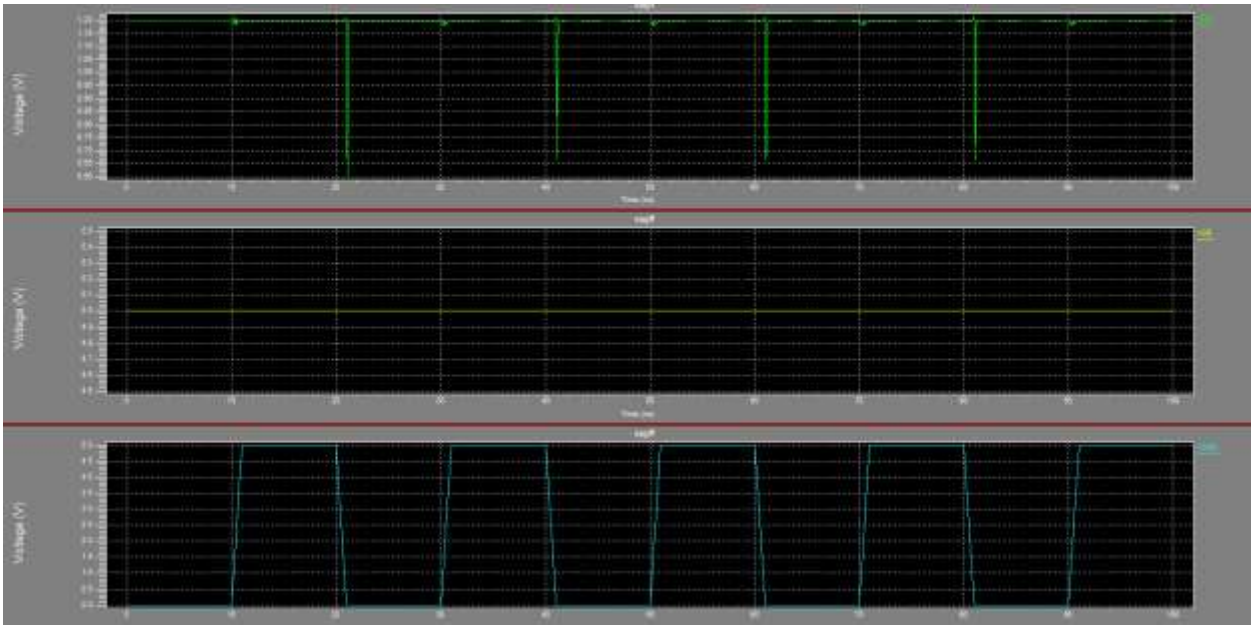


Fig 4.5 :- Output waveform for symmetric pulse generator flip flop

The absorption of power for generator of pulse that is symmetric is 2.365008e-005W.

4.4 PROPOSED DESIGN

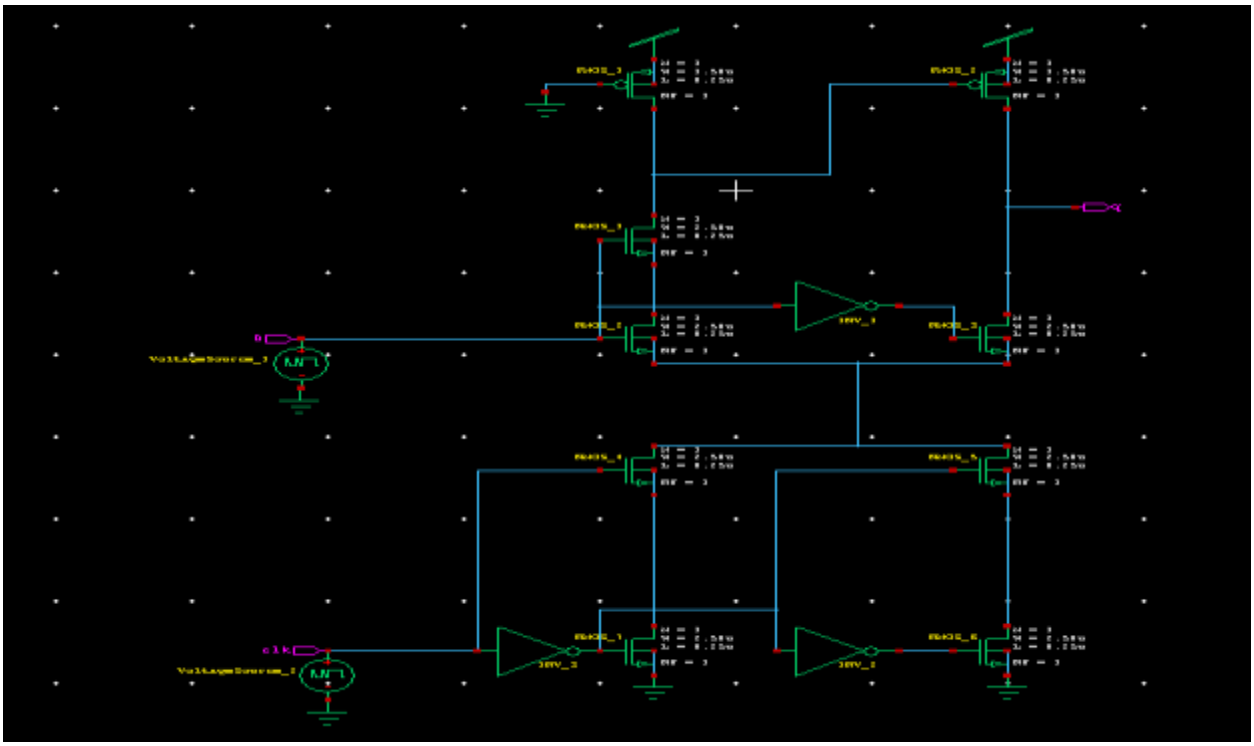


Fig 4.6 :- Suggested circuitry of CBS

Fig :- 4.7 :- Waveform of outcome for suggested CBS

4.5 COMPARISON TABLE

Circuit	Power Consumption Results
Conventional dual-edge flip-flop	3.308431e-004 watts
Dual-edge static hybrid flip-flop	1.693103e-004 watts .
Symmetric pulse generator flip-flop	2.365008e-005 watts
Proposed CBS	4.655472e-006 watts
Base paper	21 e -006 watts
Reference paper [1]	21 e -006 watts
Reference paper [4]	160.56 e-006 watts

Table 4.1 :- Table of contrast for outcome of power

CHAPTER 5

CONCLUSION & FUTURE SCOPE

5.1 CONCLUSION

In this thesis, we observed the FFs that are clocked on double edge & are segregated in three classes. Traditional DEFF copy the constituent that latches thus copying of area & enhancing the load on input. The FFs that are explicit on pulse of DE possess an external generator of pulse thus absorbs more power. This suggested CBS IP makes use of branch of clock schema of distribution for sampling of transitions of clock that eventually decrease in the quantity of transistors that are clocked & leads to less power & regulate the speed. It implies the methodology to discharge on conditions & segregate the method path to deduce the switching in redundancy & current in short circuitries. The FF of CBSIP possess minimal number of transistors that are clocked & minimal power as well. Thus it is taken as the best match for greater performance & conditions with lessen power.

5.2 FUTURE SCOPE

In this project , we can further improve performance of design circuit results . We can reduce the channel length for reduce the area and power with delay .